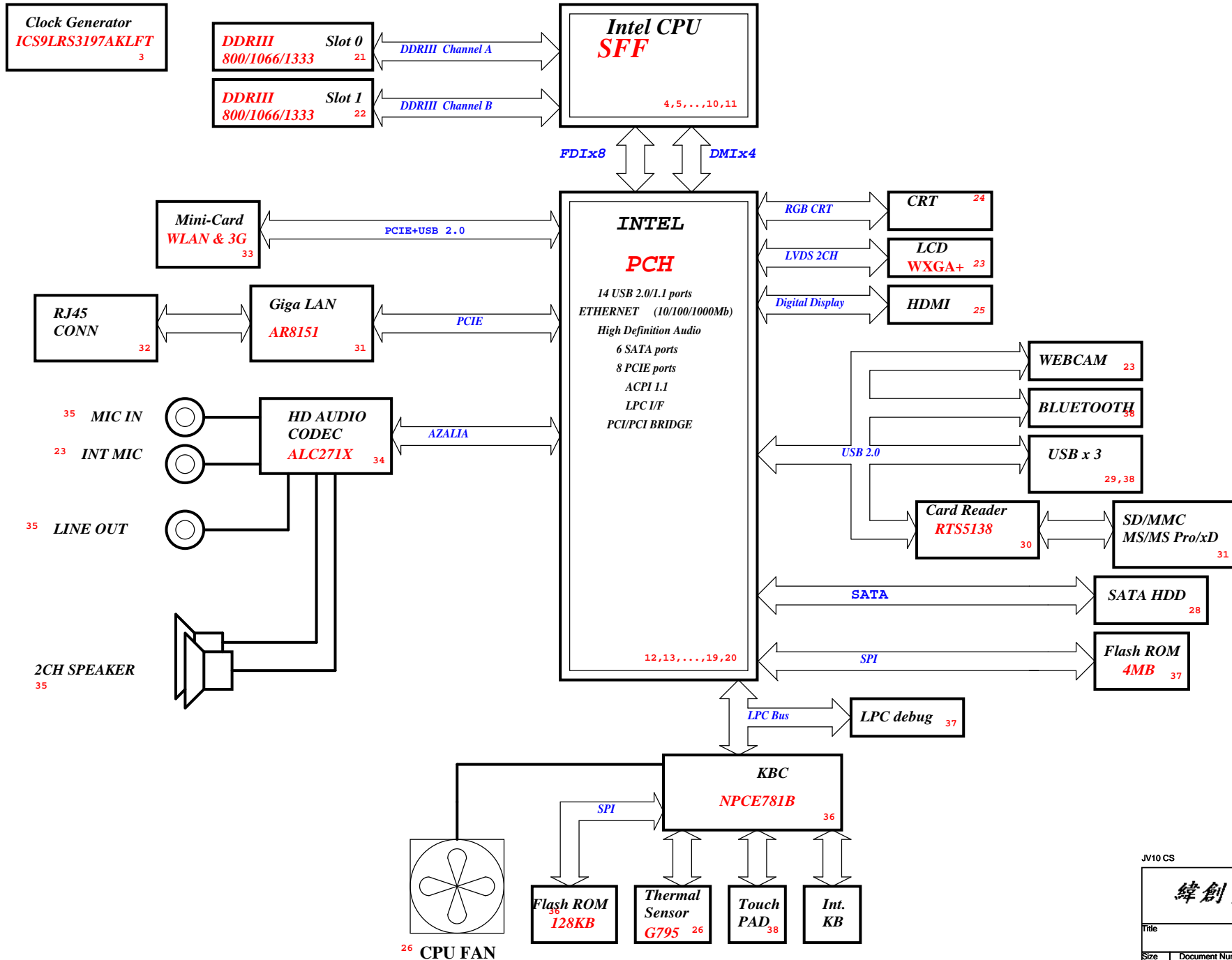


JV10-CS Block Diagram

Project code:91.4GS01.001

PCB P/N :48.4GS01.0SA

REVISION :09918-1



JV10 CS

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Taipei Hsien 221, Taiwan, R.O.C.

| Title | | |
|--------------------------------|-----------------|-----|
| Block Diagram | | |
| Size A3 | Document Number | Rev |
| | JV10-CS | -1 |
| Date: Friday, January 22, 2010 | Sheet 1 of 50 | |

PCH Strapping

| Name | Schematics Notes |
|-----------------------|---|
| SPKR | Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. |
| INIT3_3V# | Weak internal pull-down. Do not pull high. |
| GNT3#/GPIO55 | Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor). |
| INTVRMEN | High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled |
| GNT0#, GNT1# | Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. |
| GNT2#/GPIO53 | Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops). |
| GPIO33 | Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor. |
| SPI_MOSI | Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required. |
| NV_ALE | Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor. |
| NC_CLE | Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN#/GPIO[33] | Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect. |
| HDA_SDO | Weak internal pull-down. Do not pull high. |
| HDA_SYNC | Weak internal pull-down. Do not pull high. |
| GPIO15 | Weak internal pull-down. Do not pull high. |
| GPIO8 | Weak internal pull-up. Do not pull low. |
| GPIO27 | Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

PCIe Routing

| | |
|-------|-----------|
| LANE1 | LAN |
| LANE2 | MiniCard1 |
| | |

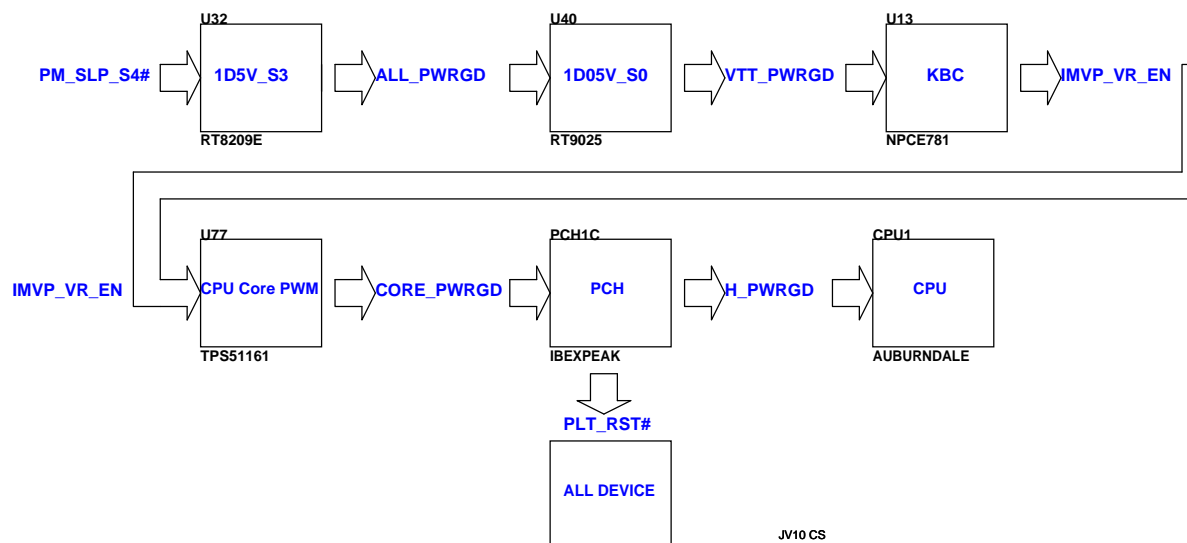
USB Table

| Pair | Device |
|------|------------|
| 0 | USB3 |
| 1 | USB2 |
| 2 | NC |
| 3 | MINICARD1 |
| 4 | WECAM |
| 5 | NC |
| 6 | NC |
| 7 | NC |
| 8 | NC |
| 9 | USB1(HS) |
| 10 | NC |
| 11 | Blue Tooth |
| 12 | MINIC2 |
| 13 | Cardreader |

Processor Strapping

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|----------|---|---|---------------|
| CFG[4] | Embedded DisplayPort Presence | 1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port. | 1 |
| CFG[3] | PCI-Express Static Lane Reversal | 1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | 1 |
| CFG[0] | PCI-Express Configuration Select | 1: Single PCI-Express Graphics 0: Bifurcation enabled | 1 |
| CFG[7] | Reserved - Temporarily used for early Clarksfield samples. | Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality. | 0 |

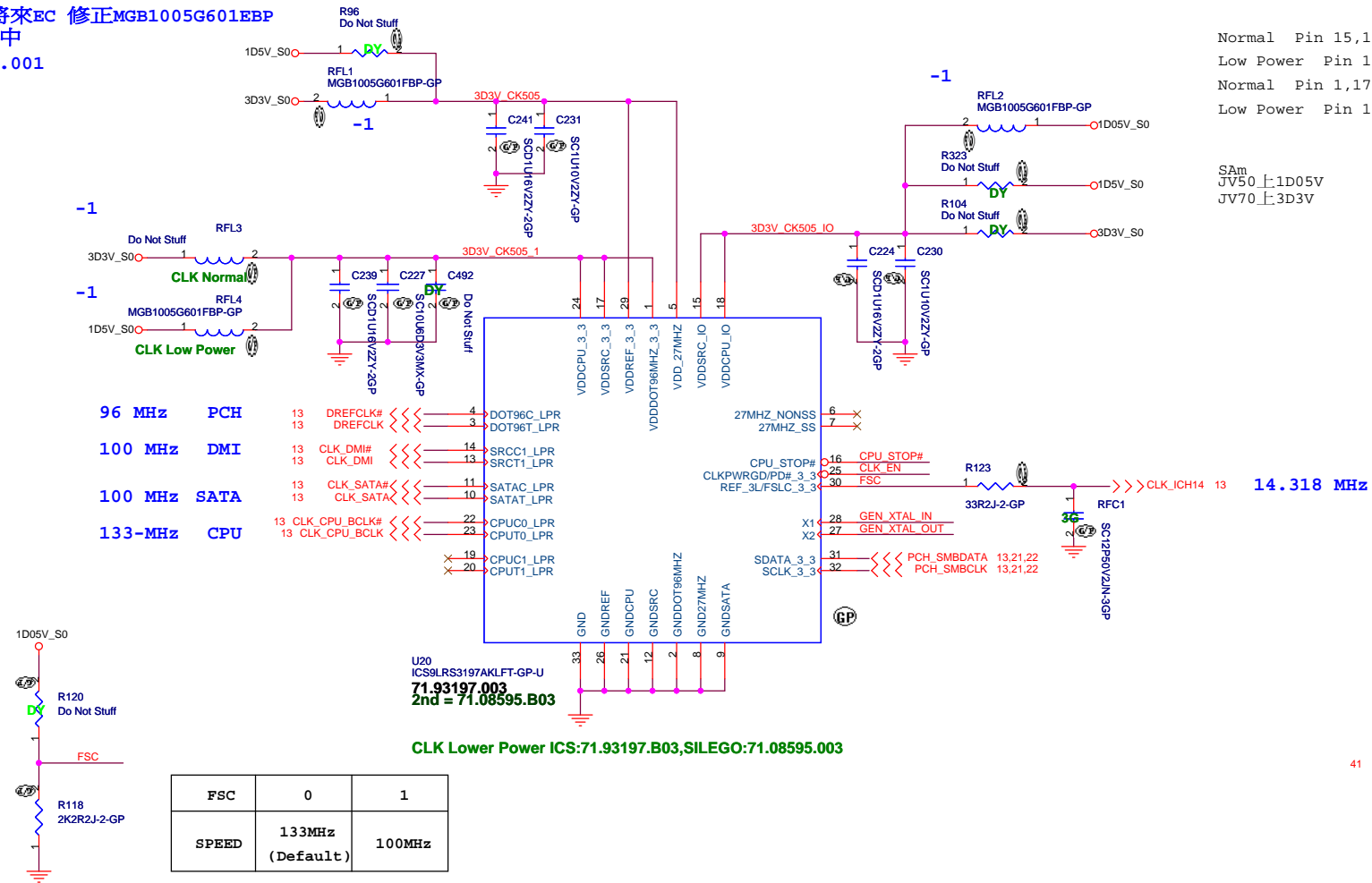
Power Sequence



JV10 CS

| | | |
|--------------------------------|--------------------------------|--|
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| Title Table of Content | | |
| Size A3 | Document Number JV10-CS | Rev -1 |
| Date: Friday, January 22, 2010 | Sheet 2 of 50 | |

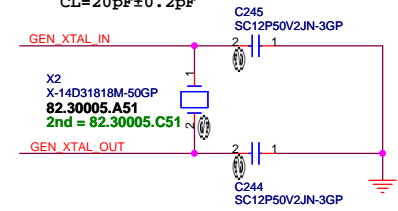
RFL1~4 將來EC 修正MGB1005G601EBP
料號申請中
68.00373.001



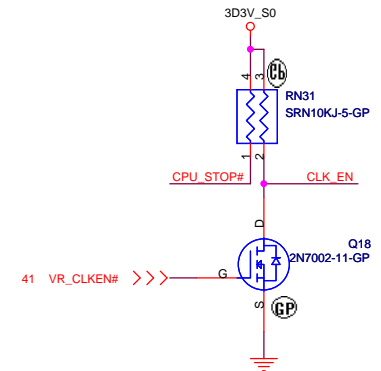
```
Normal Pin 15,18---3.3V/1.05V
Low Power Pin 15,18---1.5V/1.05V
Normal Pin 1,17,24---3.3V/1.05V
Low Power Pin 1,17,24---1.5V/1.05V
```

SAm
JV50 上1D05V
JV70 上3D3V

14.31818M HZ
CL=20pF±0.2pF



14.318 MHz

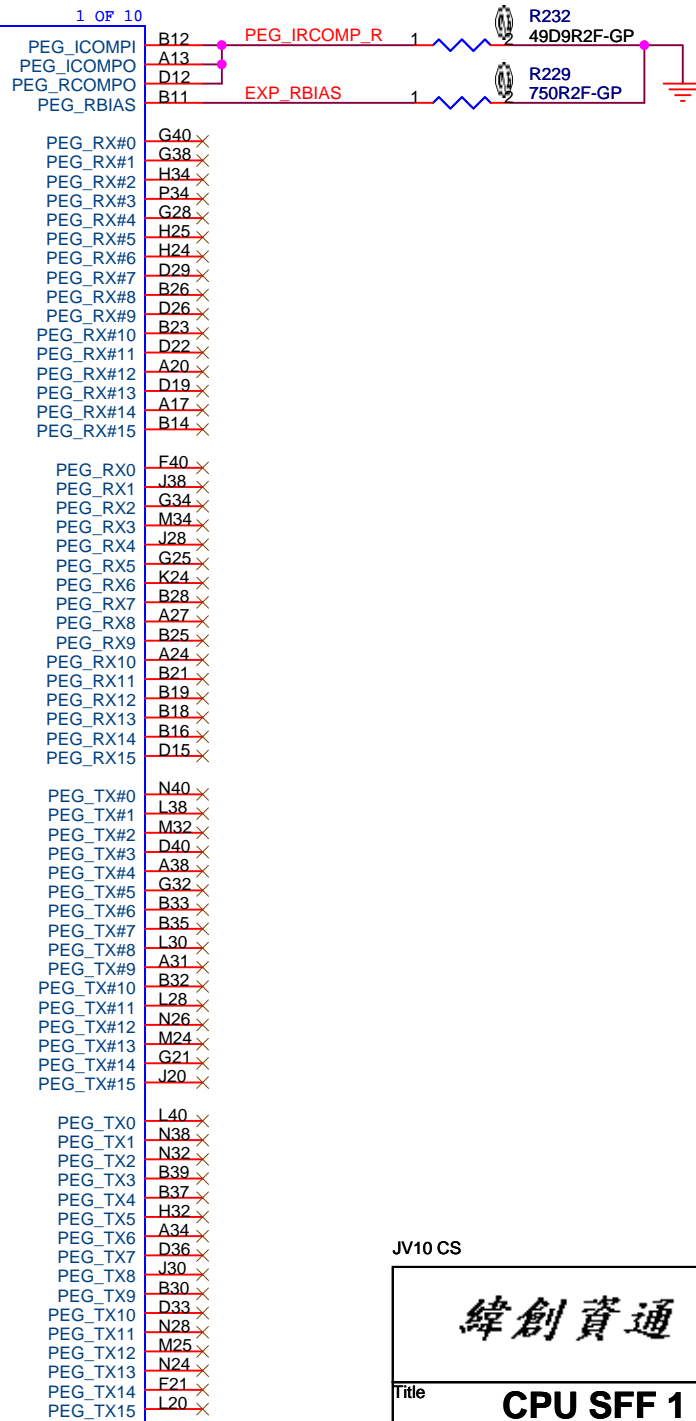
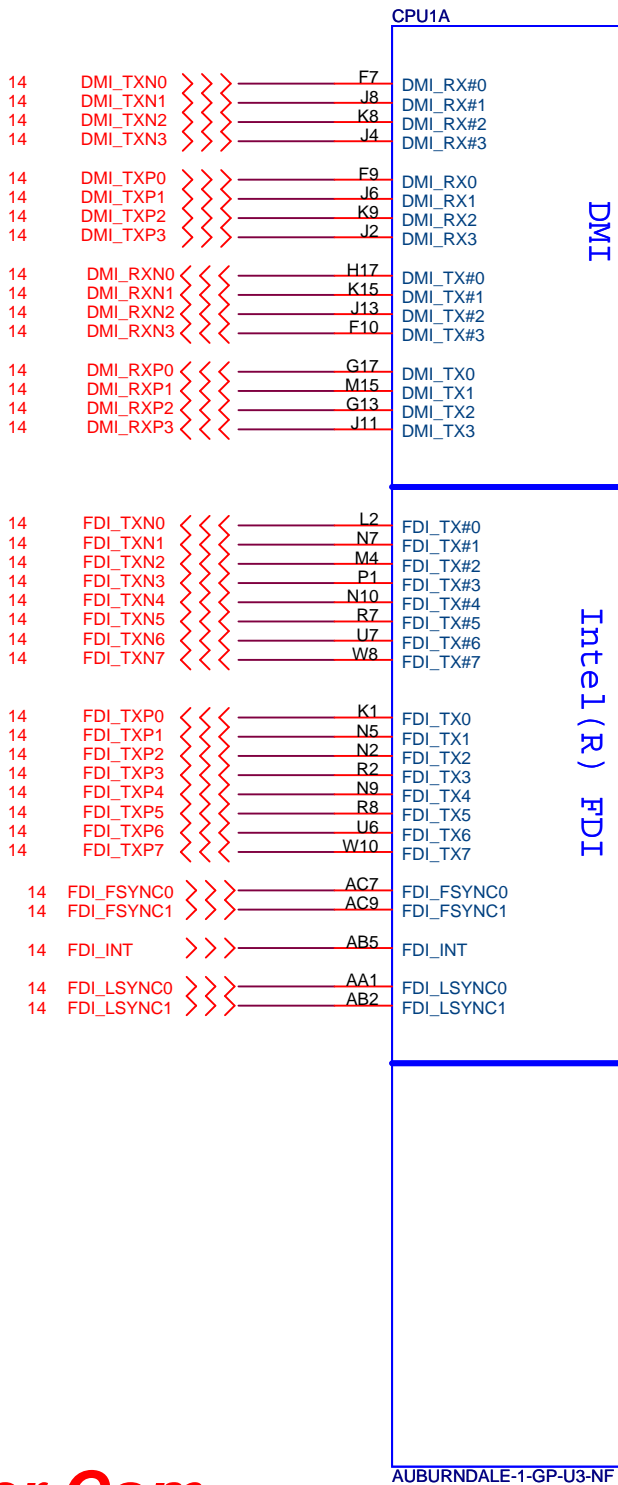


| | | |
|-------|---------------------|--------|
| FSC | 0 | 1 |
| SPEED | 133MHz (Default) | 100MHz |

JV10 CS

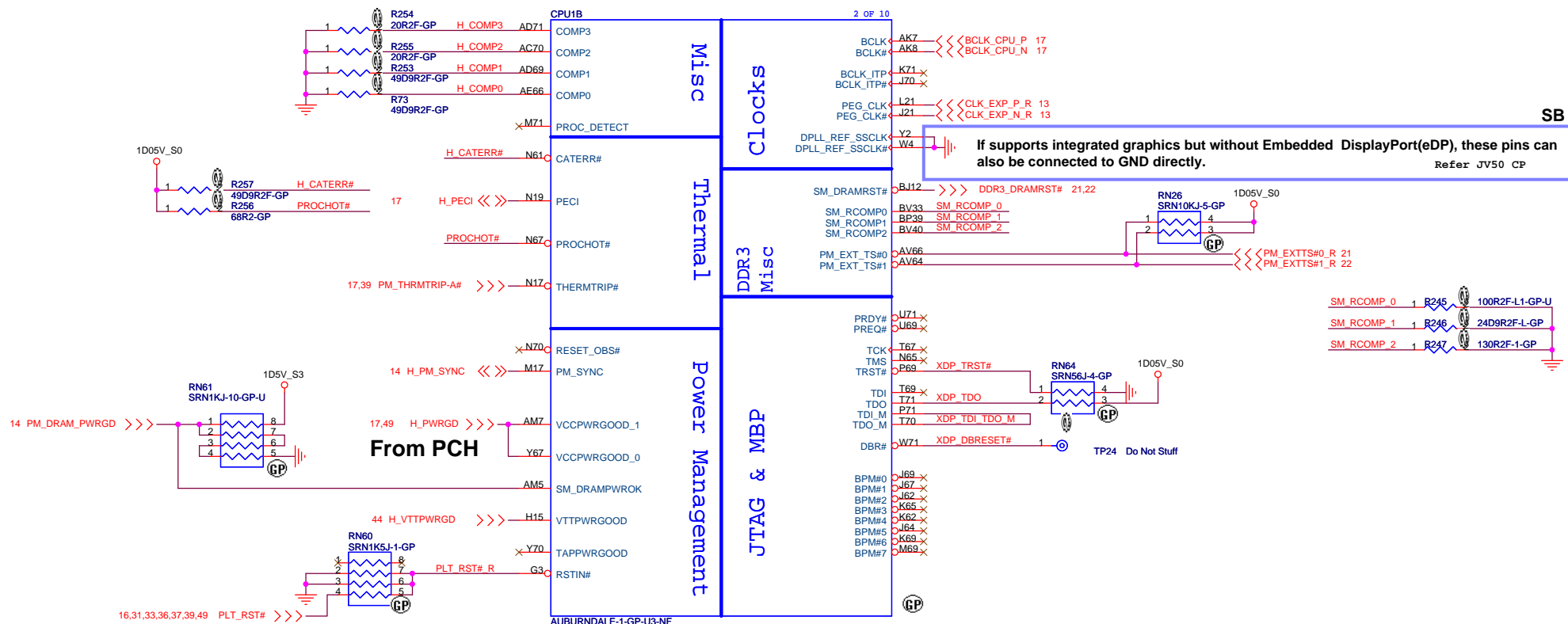
緯創資通 **Wistron Corporation**
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| | | | |
|------------------------|--------------------------|------------|-----------|
| Title | | | |
| Clock Generator | | | |
| Size Custom | Document Number | | Rev |
| | JV10-CS | | -1 |
| Date: | Friday, January 22, 2010 | Sheet 3 of | 50 |



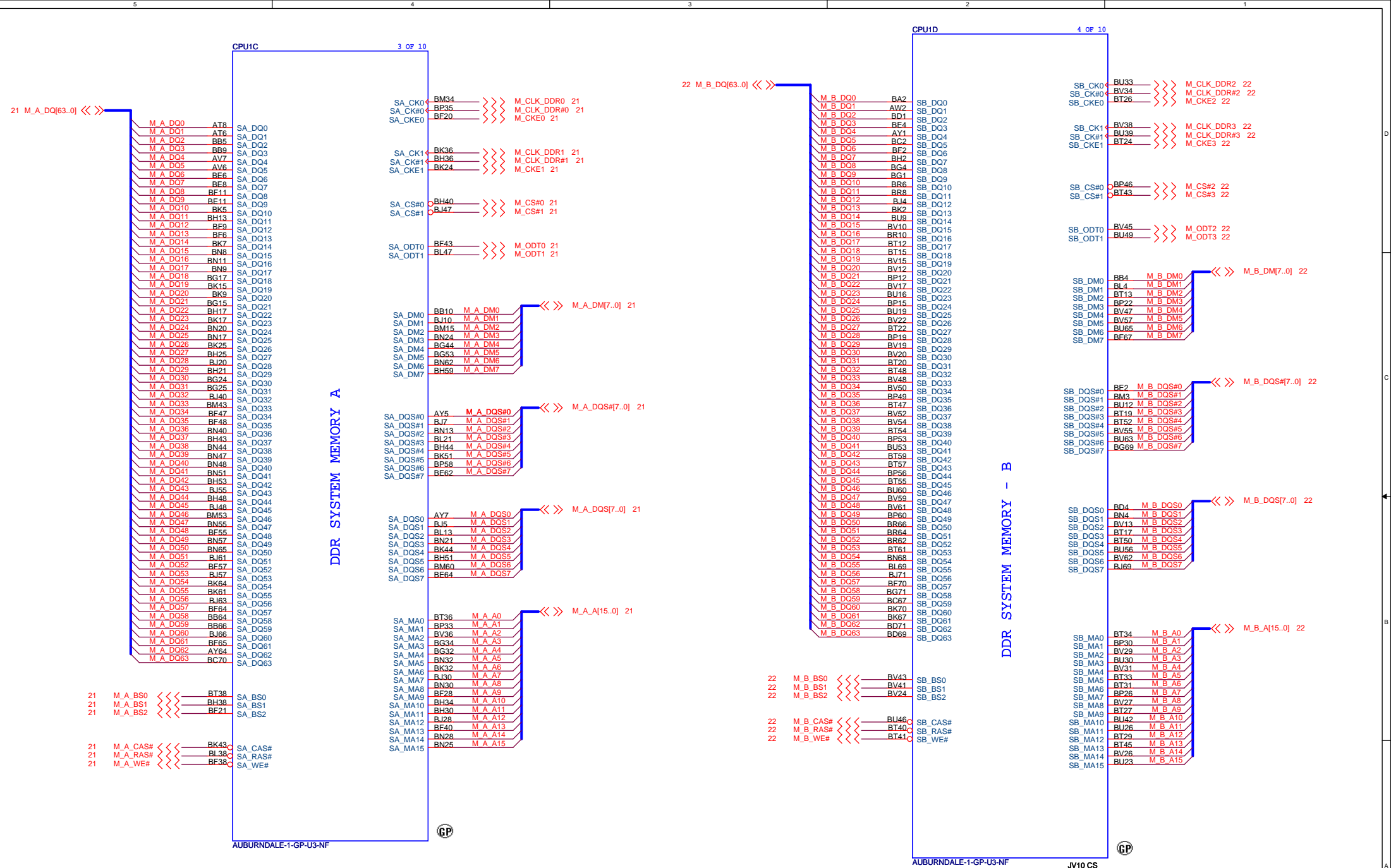
JV10 CS

| | | | | | |
|--|-------------------------|---------|----------------------------|-------|--------|
| 緯創資通 | | | Wistron Corporation | | |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | | | | |
| Title CPU SFF 1 of 8(DMI/FDI/PEG) | | | | | |
| Size A4 | Document Number JV10-CS | | | | Rev -1 |
| Date: Friday, January 22, 2010 | | Sheet 4 | | of 50 | |

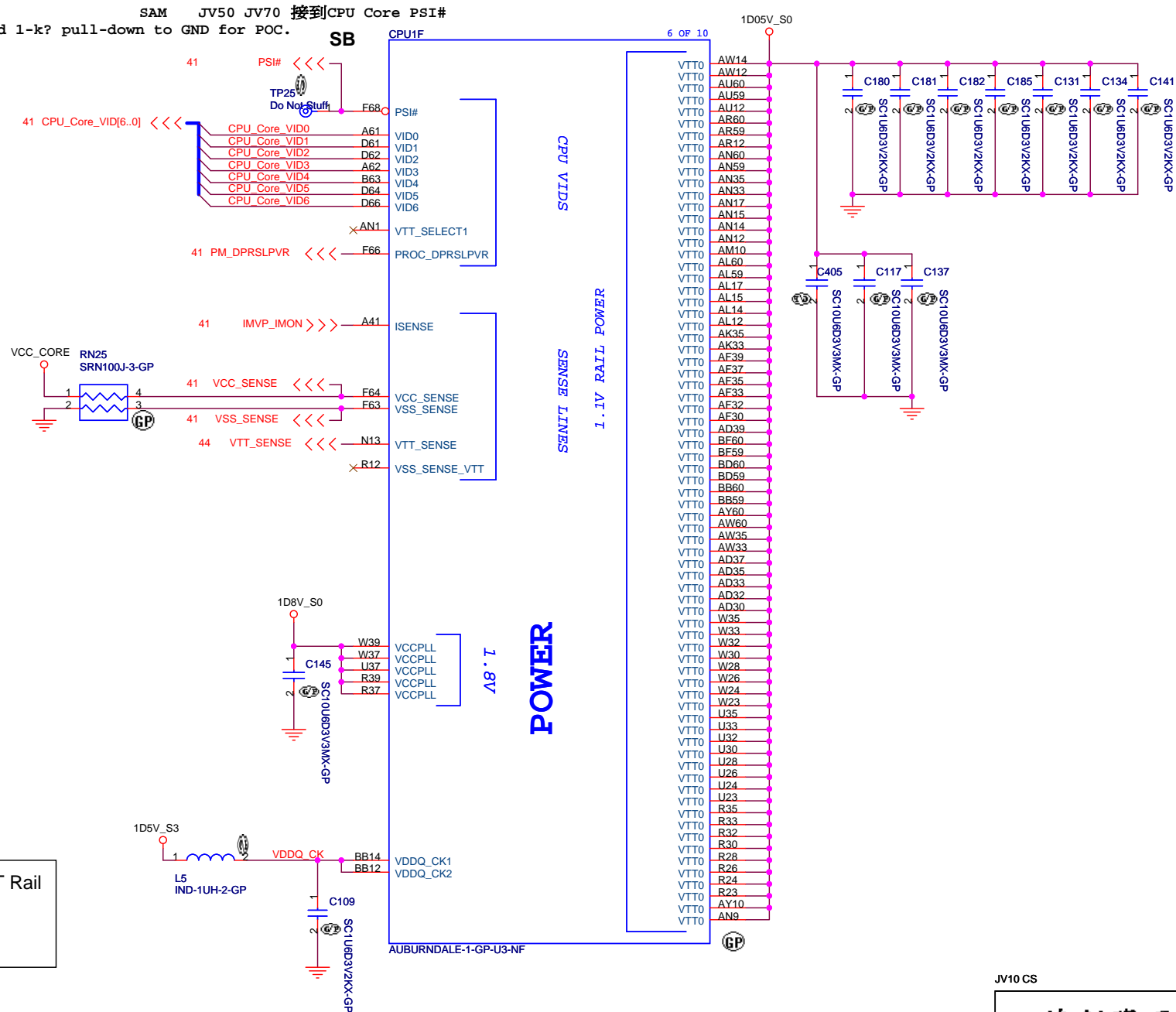


JV10 CS

| | |
|--|-----------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | |
| CPU SFF 2 of 8(CLK/Thermal) | |
| Size | Document Number |
| Custom | JV10-CS |
| Date: Friday, January 22, 2010 | Sheet 5 of 50 |
| Rev | |
| -1 | |



check list
1-k? pull-up to VTT and 1-k? pull-down to GND for POC.
1D05V_VTT



Please note that the VTT Rail
Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V

JV10 CS

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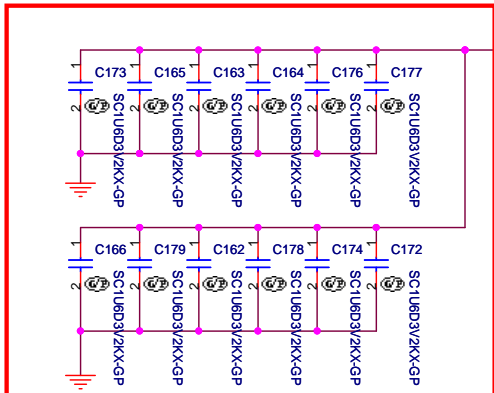
Title CPU SFF 4 of 8(Power/VTT)

Size Document Number JV10-CS

Rev
-1

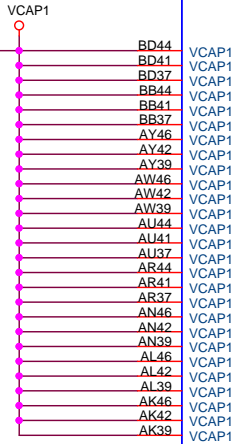
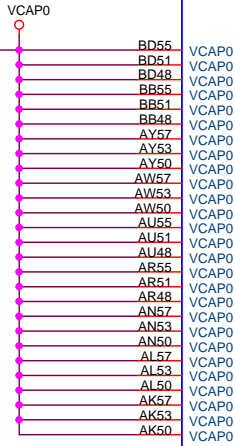
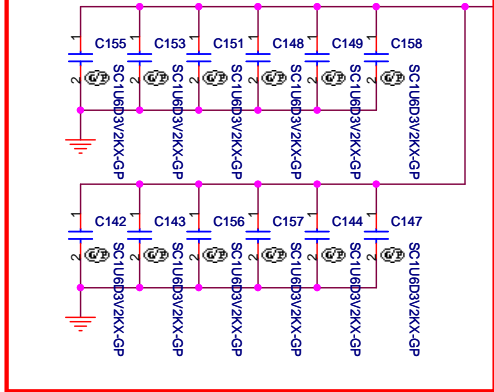
Date: Friday, January 22, 2010

Sheet 7 of 50



Sam

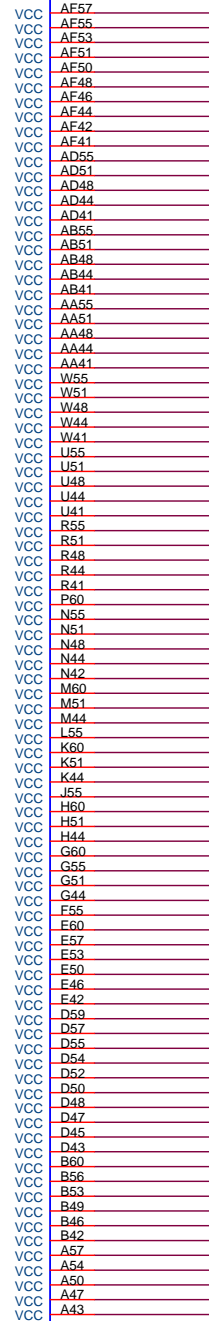
Processor package decoupling -
DO NOT connect to any power rail



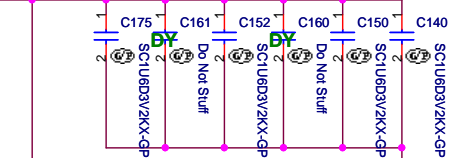
POWER

CPU CORE SUPPLY

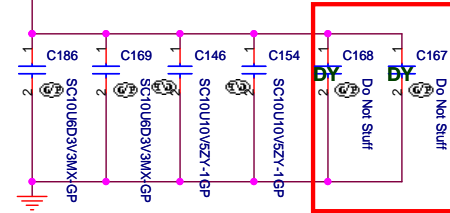
AUBURNDAL-1-GP-U3-NF



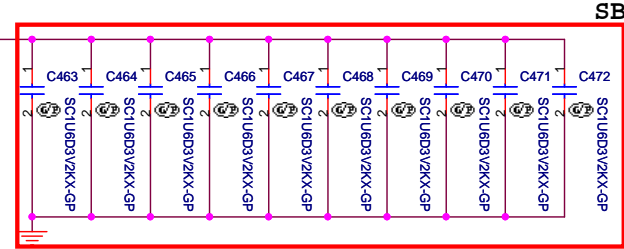
VCC_CORE



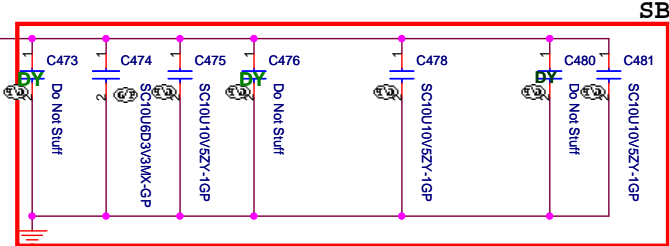
modify C160 C161



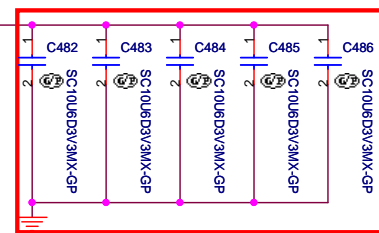
modify C167 C168



SB



SB



SB

modify C477 C479 C476 C473

JV10 CS

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Title **CPU SFF 6 of 8(CPUCORE)**

Size Document Number **JV10-CS** Rev **-1**

Date: Friday, January 22, 2010 Sheet 9 of 50

CPU1E

5 OF 10

RSVD#W66
RSVD#W64W66
W64RSVD#AC69
RSVD#AC71AC69
AC71RSVD#AA71
RSVD#AA69AA71
AA69RSVD#R66
RSVD#R64R66
R64RSVD_NCTF#BT5
RSDV_NCTF#BR5BT5
BR5RSDV_NCTF#BV6
RSDV_NCTF#BV8BV6
BV8RSVD#AV69
RSVD#AK71AV69
AK71RSVD#AN69
RSVD#AP66AN69
AP66RSVD#AH66
RSVD#AK66AH66
AK66RSVD#AR71
RSVD#AM66AR71
AM66RSVD#AK69
RSVD#AU71AK69
AU71RSVD#AT70
RSVD#AR69AT70
AR69RSVD#AU69
RSVD#AT67AU69
AT67RSVD#AV4
RSVD#AU2AV4
AU2RSVD#BE69
RSVD#BE71BE69
BE71NCTF_DC_TEST#BV71
NCTF_DC_TEST#BV69BV71
BV69NCTF_DC_TEST#BV68
NCTF_DC_TEST#BV5BV68
BV5NCTF_DC_TEST#BV3
NCTF_DC_TEST#BV1BV3
BV1NCTF_DC_TEST#BT71
DC_TEST_BT69BT71
BT69DC_TEST_BT3
NCTF_DC_TEST#BT1BT3
BT1NCTF_DC_TEST#BR71
NCTF_DC_TEST#BR1BR71
BR1NCTF_DC_TEST#E71
NCTF_DC_TEST#E1E71
E1NCTF_DC_TEST#C71
DC_TEST_C69C71
C69NCTF_DC_TEST#C3
NCTF_DC_TEST#A71C3
A71NCTF_DC_TEST#A69
NCTF_DC_TEST#A68A69
A68

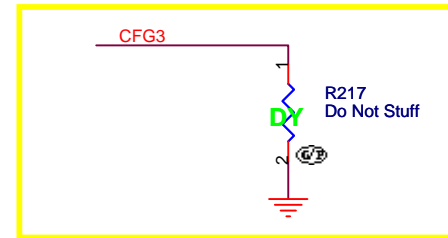
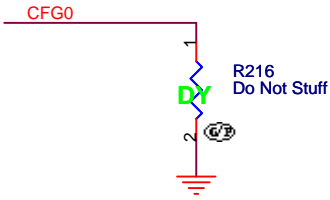
NCTF_DC_TEST#A5

A5

NCTF TEST PIN:

A5, A68, A69, A71, C3, C71, E1, E71, BR1, BR71, BT1, BT71, BV1, BV3, BV5, BV68, BV69, BV71

AUBURNDALE-1-GP-U3-NF



PCI-Express Configuration Select

CFG0

1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

CFG3

1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

JV10 CS

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Title CPU SFF 7 of 8(REERVED)

Size
A4

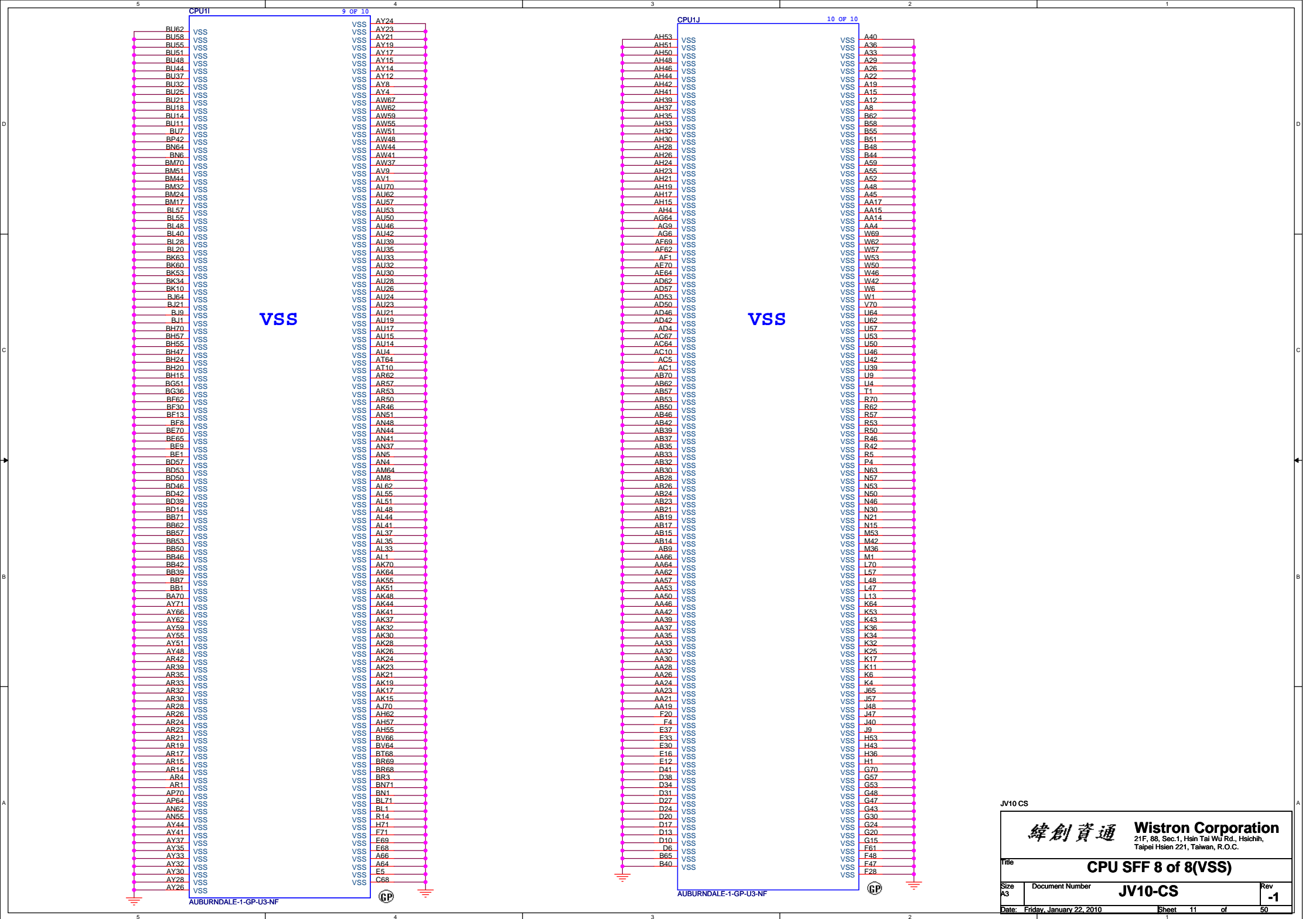
Document Number

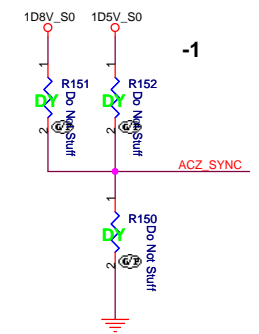
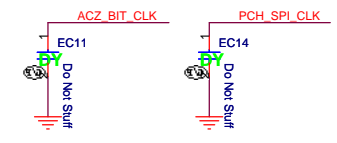
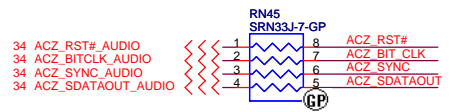
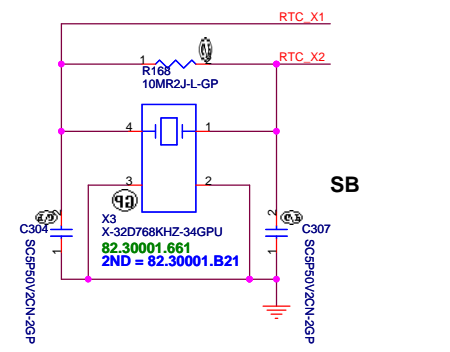
JV10-CS

Rev
-1

Date: Friday, January 22, 2010

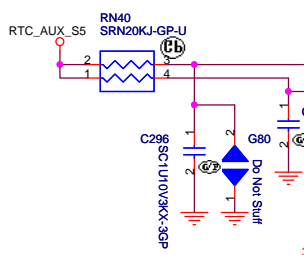
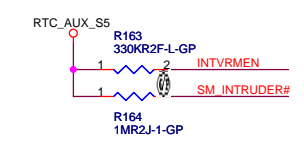
Sheet 10 of 50



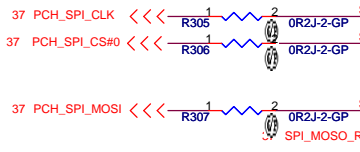
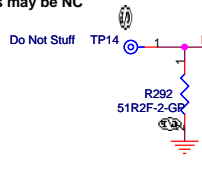


If reserve 1.5/1.8V option for VCCVRM. Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).

WWW.AliSaler.Com

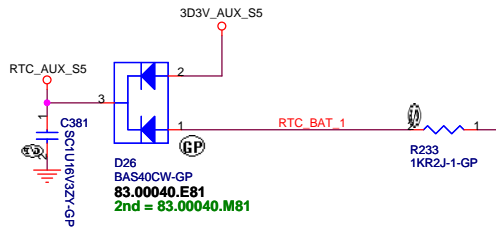


When unused all JTAG pins may be NC



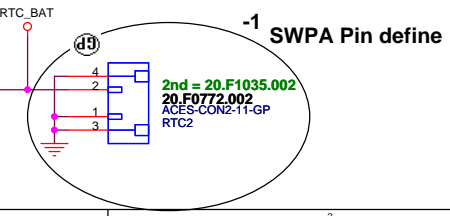
SPI_CS#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

RTC CONN

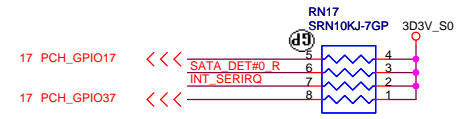
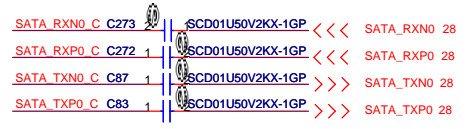
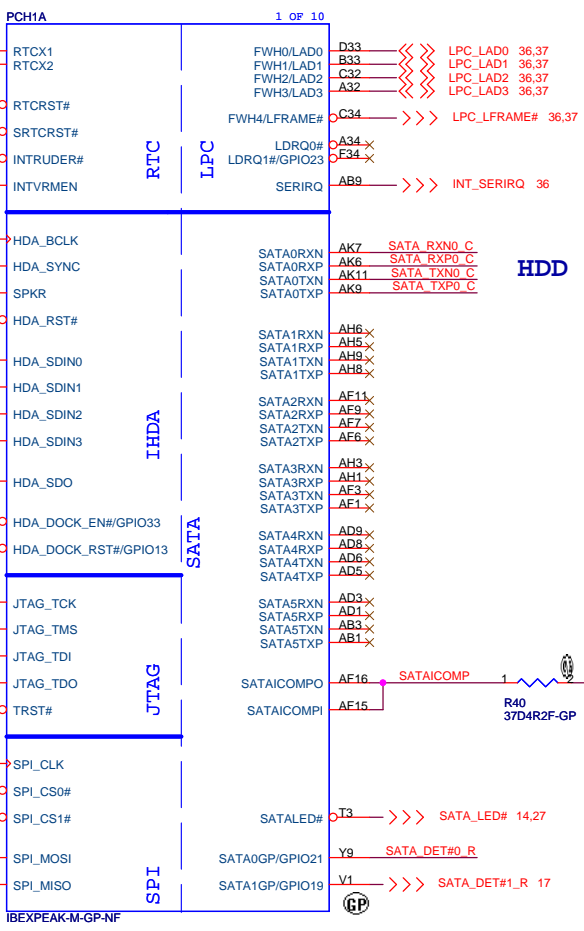


23.25218.001

Pin define 要換,確認connector part number



| | | |
|--|-------------|-------------|
| Integrated VccSus1_05,VccSus1_5,VccCL1_5 | | |
| INTVRMEN | High=Enable | Low=Disable |
| Integrated VccLan1_05VccCL1_05 | | |
| LAN100_SLP | High=Enable | Low=Disable |



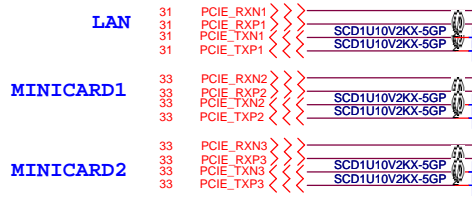
JV10 CS

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Title **PCH 1 of 9(SATA/RTC/HDA)**

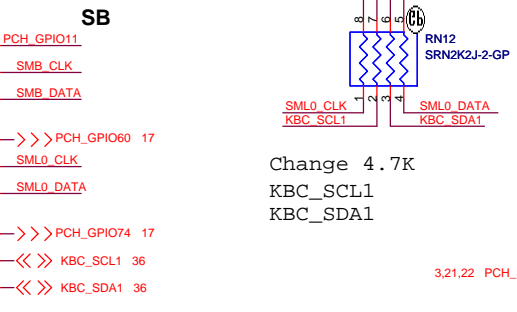
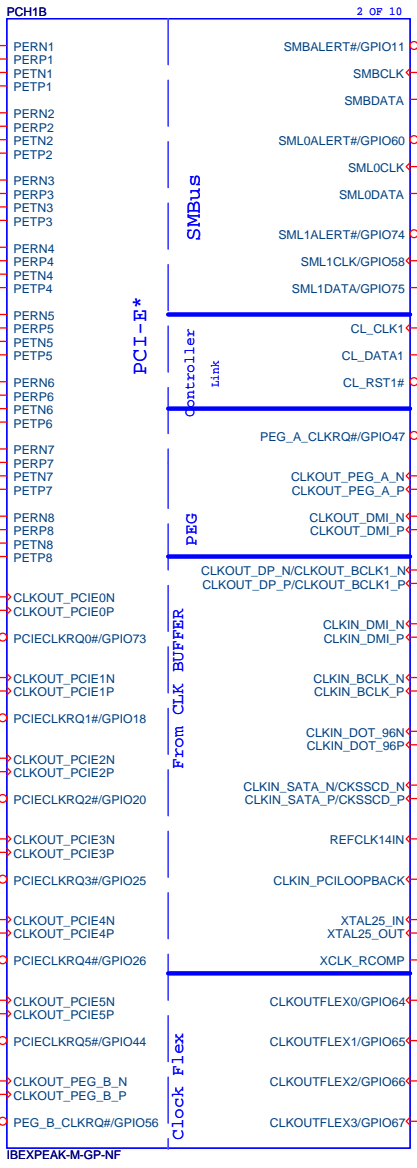
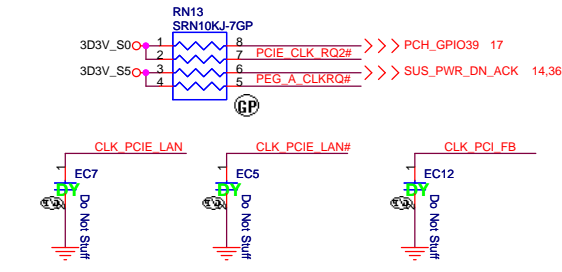
Size A3 Document Number **JV10-CS** Rev **-1**

Date: Friday, January 22, 2010 Sheet 12 of 50



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

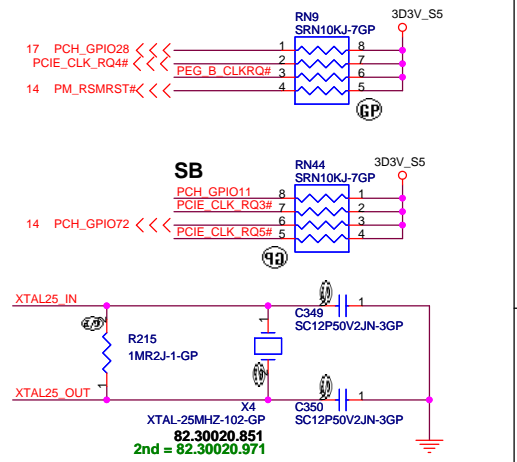
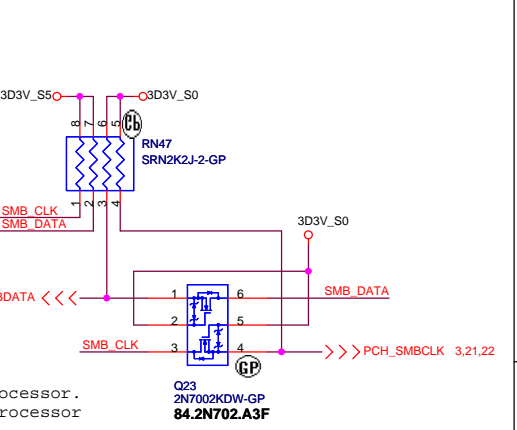
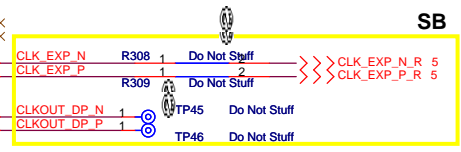


check list

100-MHz differential clock from PCH to processor.

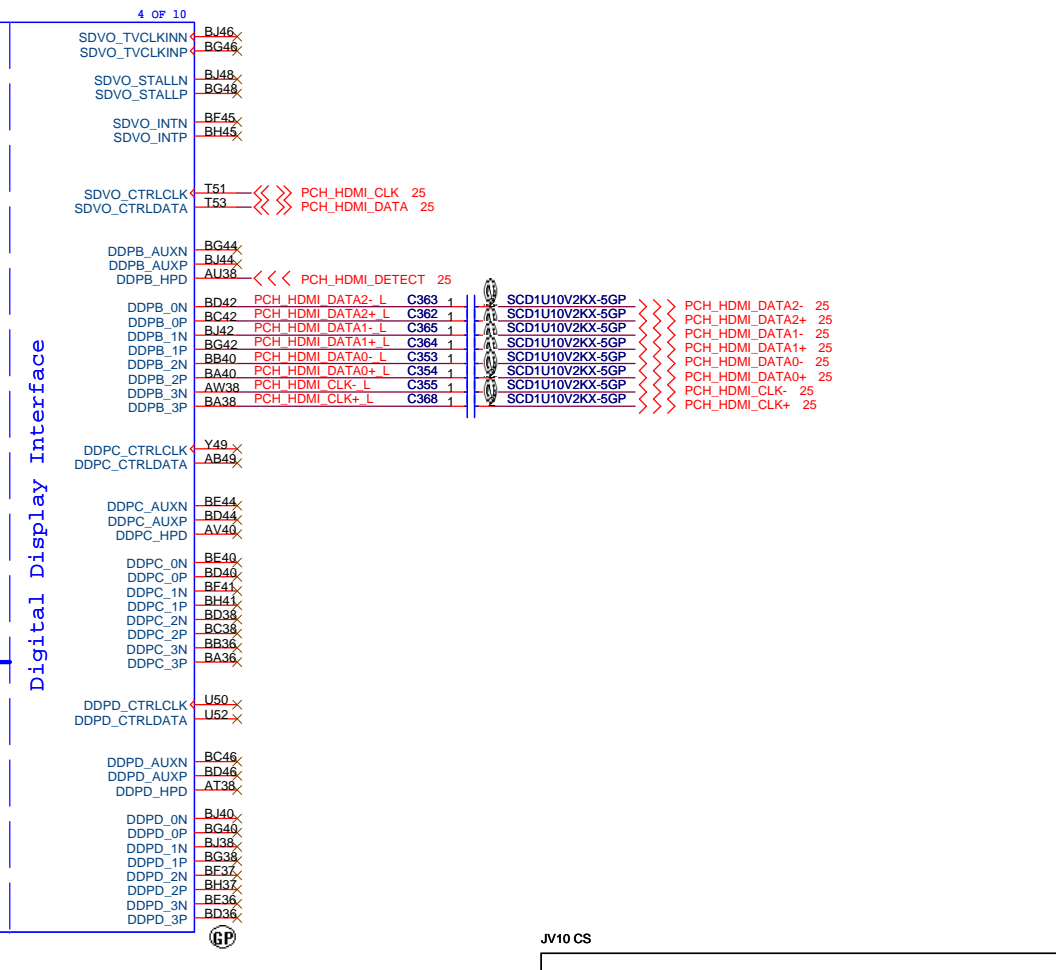
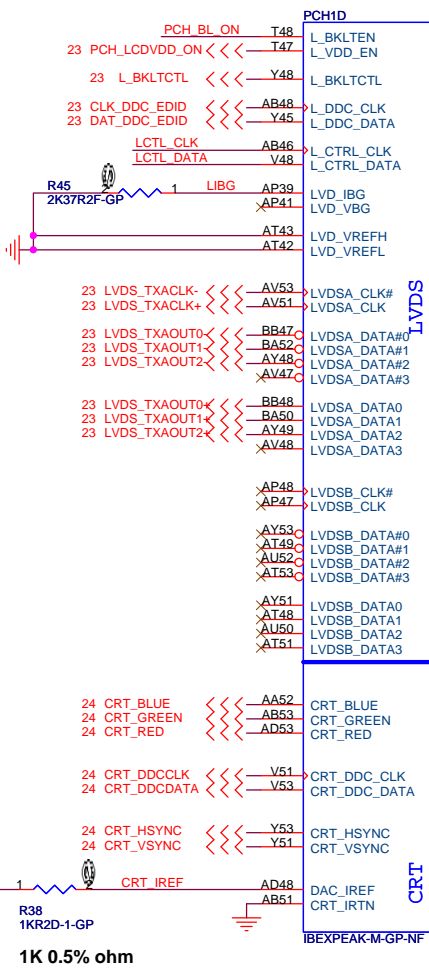
Connect to PEG_CLK#/PEG_CLK pins of the processor

沒電阻



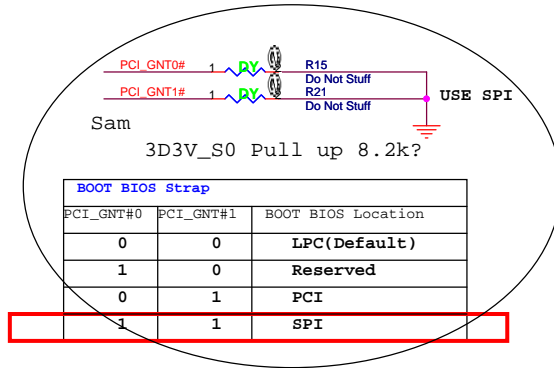
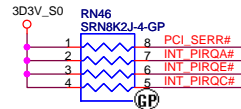
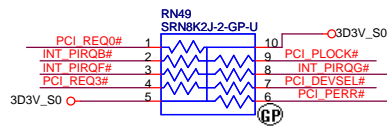
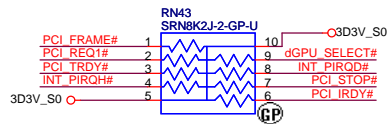


SB



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| | | | | | | | |
|--------------------------------|-----------------|--|--|--------------------------------|--|-----------|--|
| Title | | | | PCH 4 of 9(LVDS/CRT/DP) | | | |
| Size | Document Number | | | | | Rev | |
| Custom | JV10-CS | | | | | -1 | |
| Date: Friday, January 22, 2010 | | | | Sheet 15 of 50 | | | |



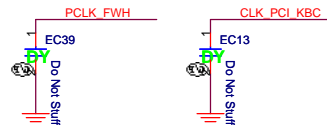
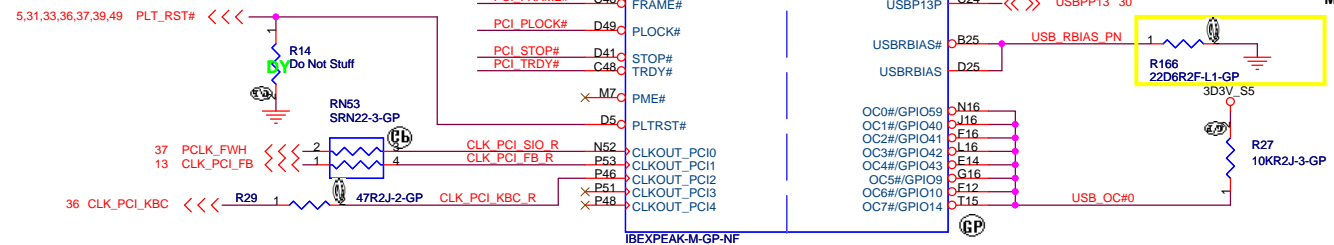
These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

USB Table

| Pair | Device |
|------|------------|
| 0 | USB3 |
| 1 | USB2 |
| 2 | NC |
| 3 | MINICARD1 |
| 4 | WECAM |
| 5 | NC |
| 6 | NC |
| 7 | NC |
| 8 | 3G |
| 9 | USB1(HS) |
| 10 | NC |
| 11 | Blue Tooth |
| 12 | MINIC2(3G) |
| 13 | Cardreader |

SB Modify SIV USB report



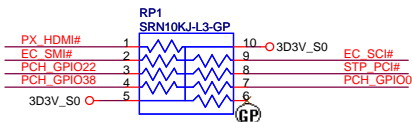
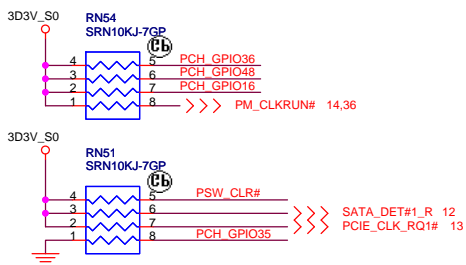
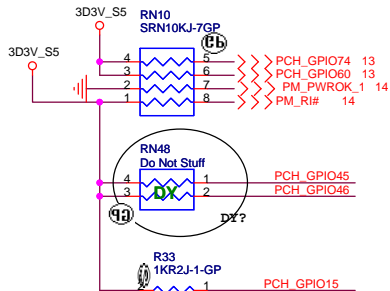
JV10 CS

| | |
|---|--------------------------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title PCH 5 of 9(PCI/USB) | |
| Size A3 | Document Number JV10-CS |
| Date: Friday, January 22, 2010 | Sheet 16 of 50 |
| Rev -1 | |

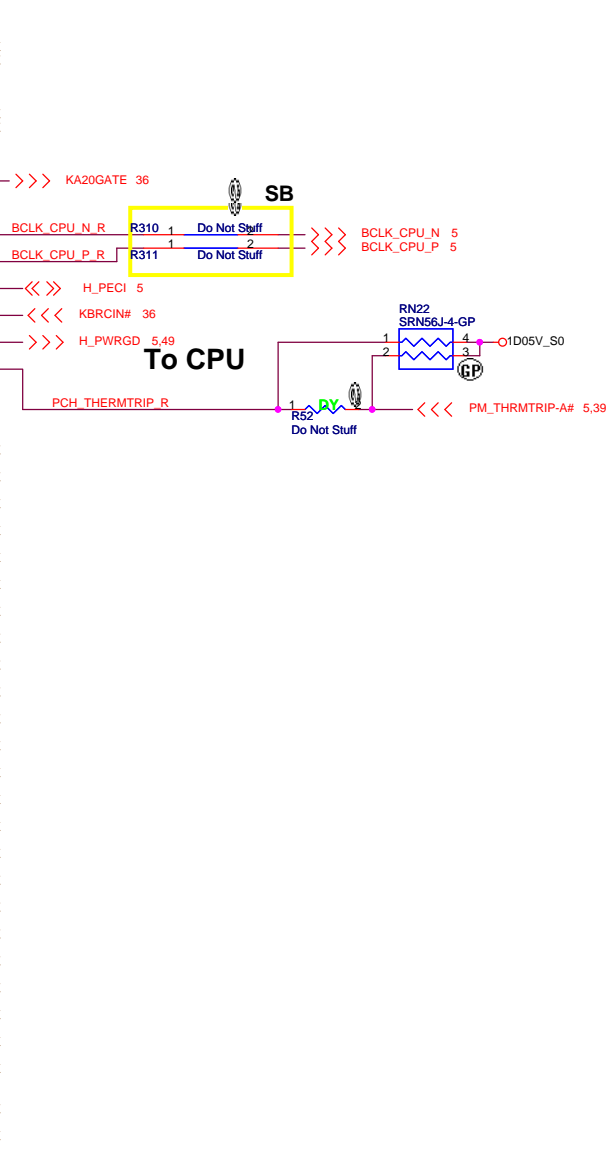
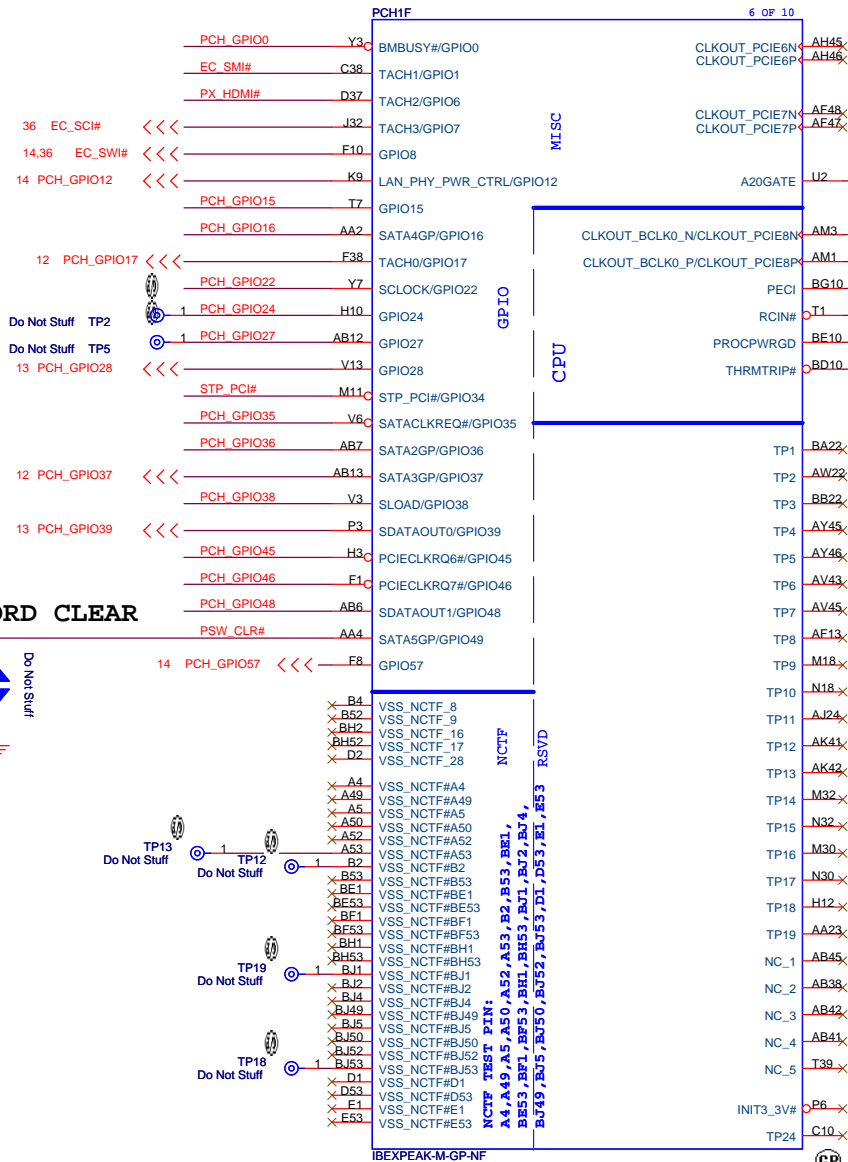
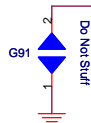
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



PASSWORD CLEAR



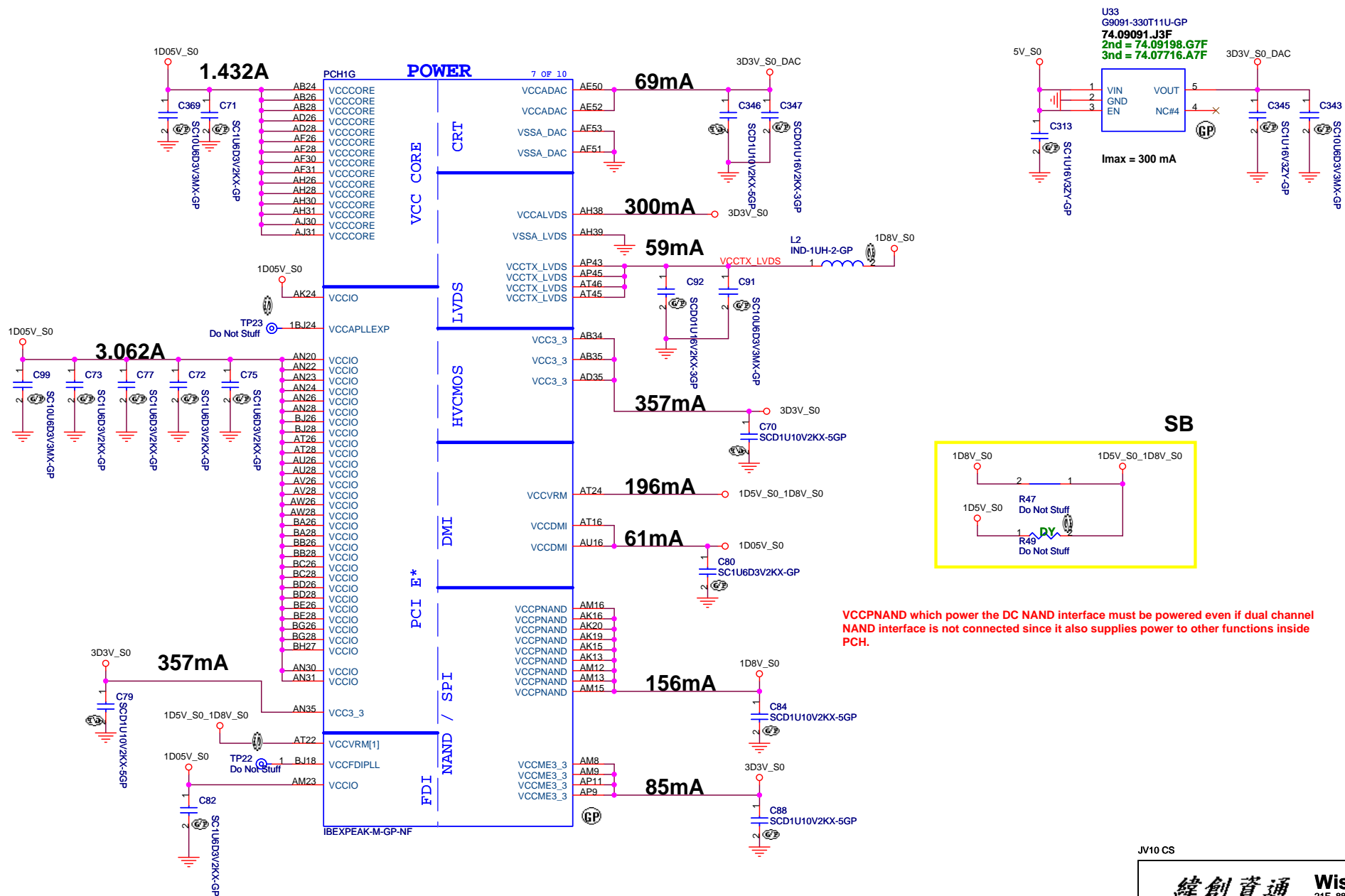
JV10 CS

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title PCH 6 of 9(GPIO/RSVD)

Size A3 Document Number JV10-CS Rev -1

Date: Friday, January 22, 2010 Sheet 17 of 50



JV10 CS

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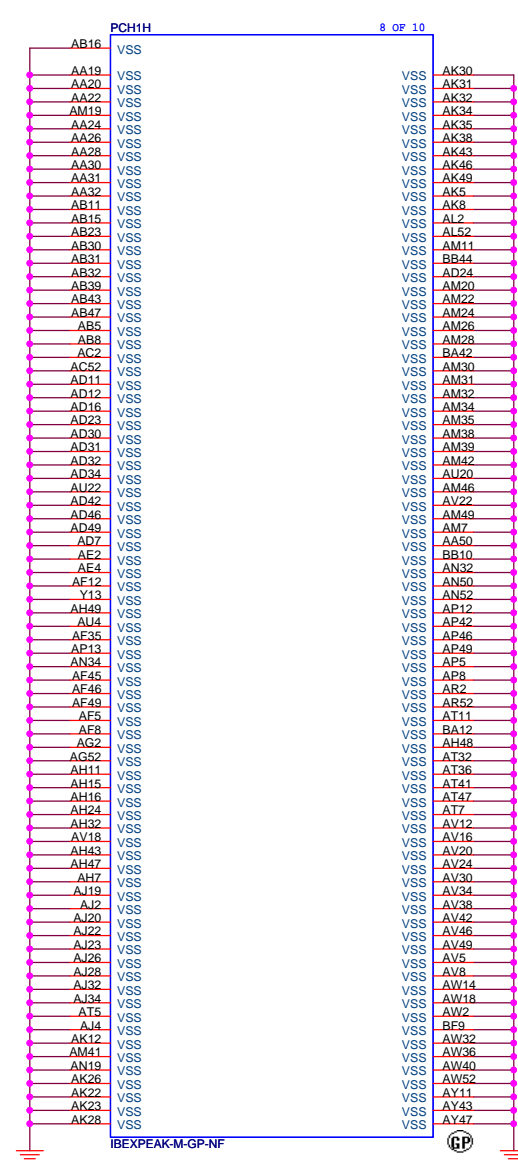
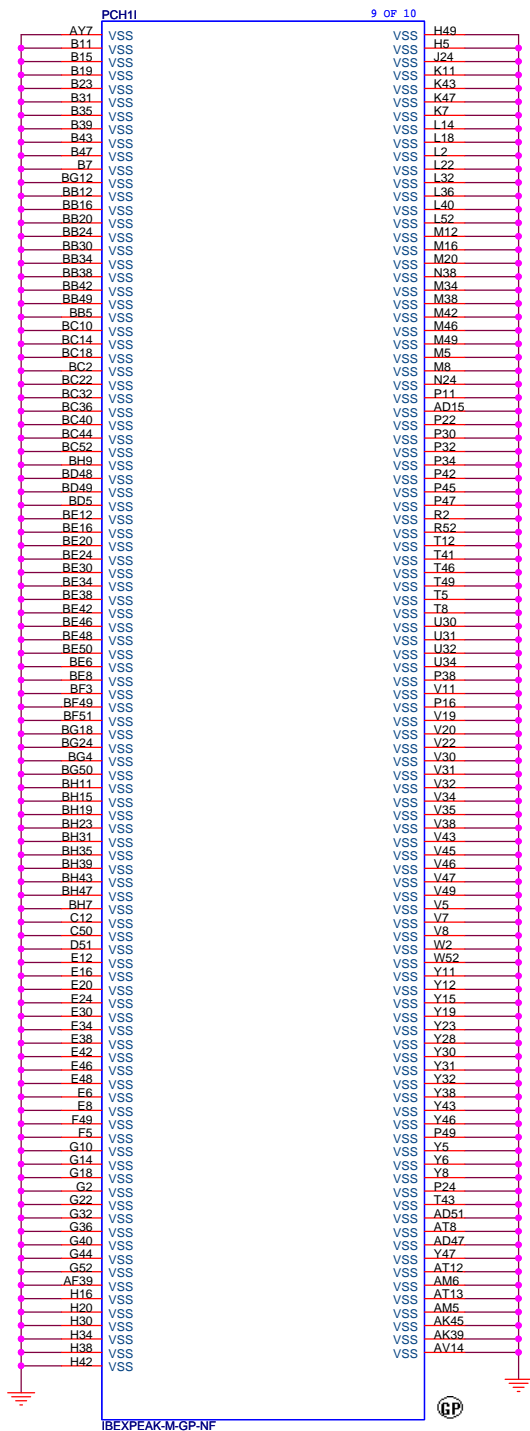
Title **PCH 7 of 9(PWR/VCORE/LVDS)**

Size Document Number **JV10-CS**

Date: Friday, January 22, 2010

Sheet 18 of 50

Rev -1



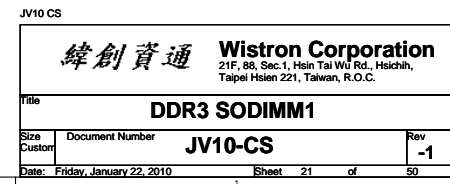
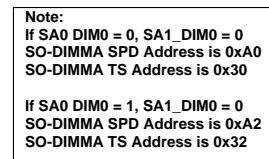
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

偉創資通

Title: **PCH 9 of 9(VSS)**

Size A3 Document Number **JV10-CS** Rev **-1**

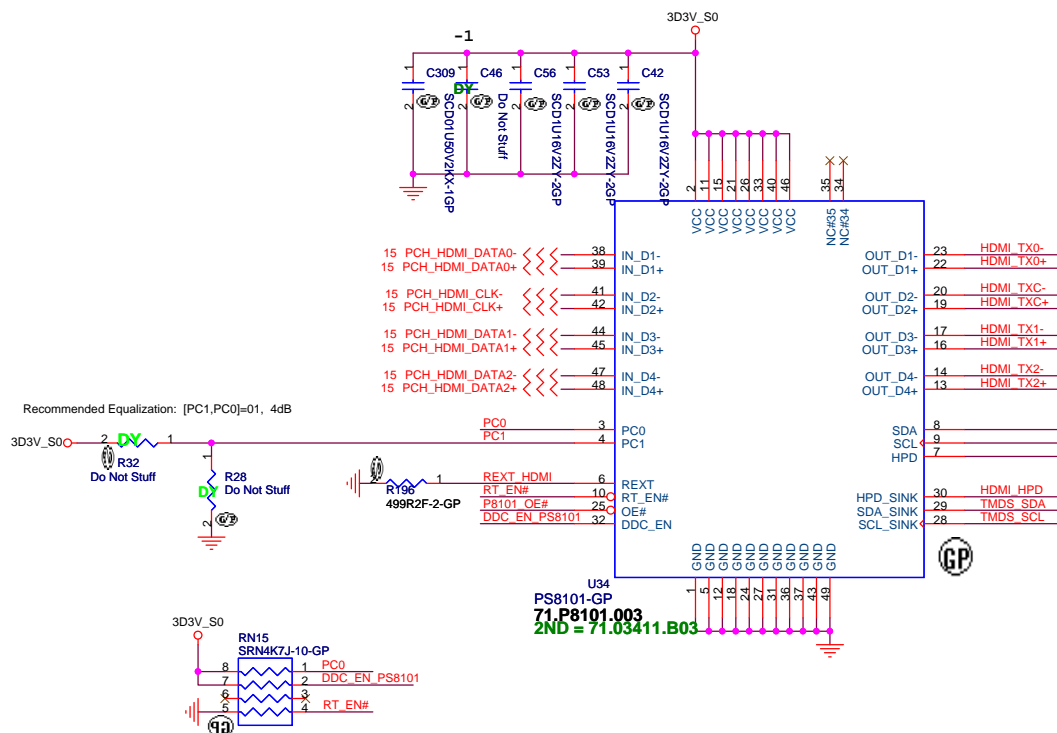
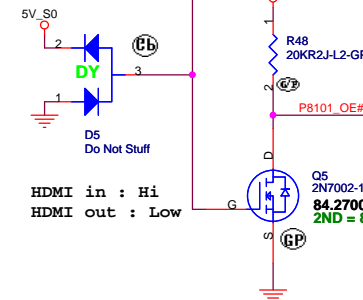
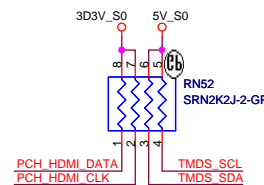
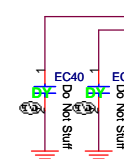
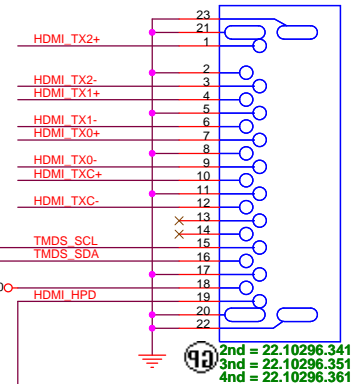
Date: Friday, January 22, 2010 Sheet 20 of 50



HDMI CONNECTOR

HDMI1
SKT-HDMI19P-20-GP-U
22.10296.051

- Pin 1 TMDS Data2+
- Pin 2 TMDS Data2 Shield
- Pin 3 TMDS Data2-
- Pin 4 TMDS Data1+
- Pin 5 TMDS Data1 Shield
- Pin 6 TMDS Data1-
- Pin 7 TMDS Data0+
- Pin 8 TMDS Data0 Shield
- Pin 9 TMDS Data0-
- Pin 10 TMDS Clock+
- Pin 11 TMDS Clock Shield
- Pin 12 TMDS Clock-
- Pin 13 CEC
- Pin 14 Reserved (N.C. on device)
- Pin 15 SCL
- Pin 16 SDA
- Pin 17 DDC/CEC Ground
- Pin 18 +5 V Power (max 50 mA)
- Pin 19 Hot Plug Detect

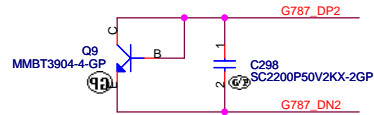


JV10 CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

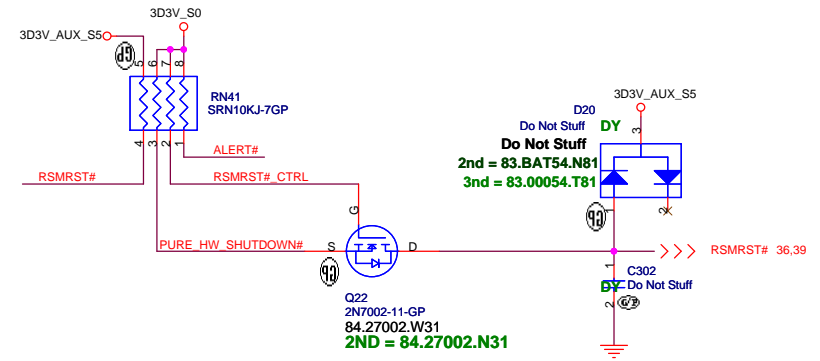
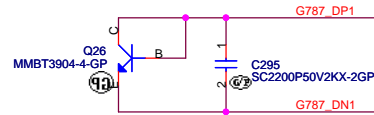
| Title | | |
|--------------------------------|-----------------|----------------|
| HDMI conn | | |
| Size | Document Number | Rev |
| Custom | JV10-CS | -1 |
| Date: Friday, January 22, 2010 | | Sheet 25 of 50 |

For T8 thermal diode



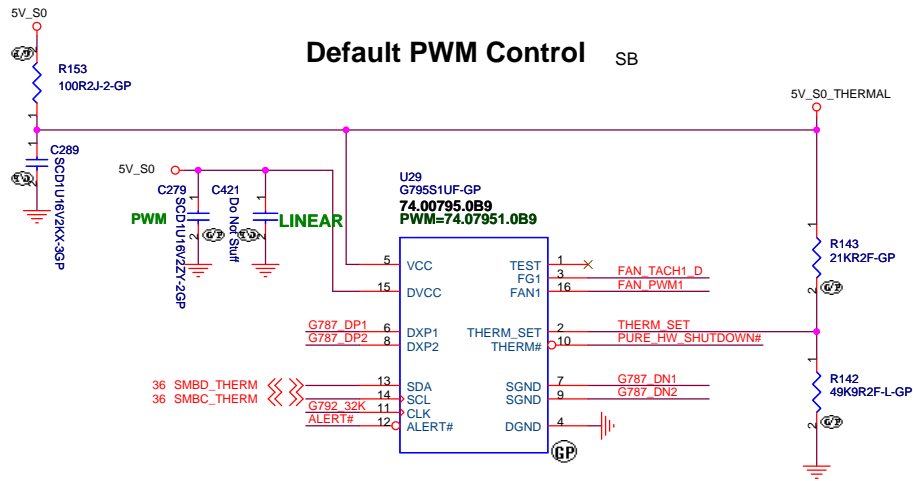
C298& C295 CLOSE to G795

For System thermal diode



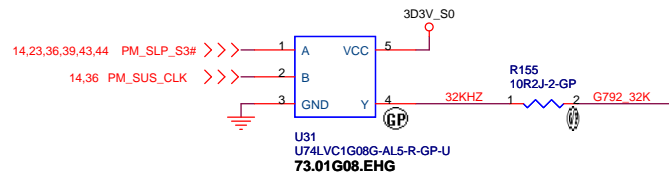
Default PWM Control

SB



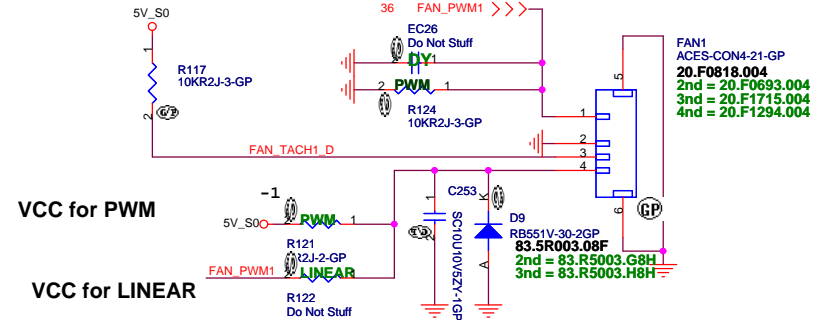
$$T8=90C$$

$$THERM_SET = [(Tset-72) \times 0.02+0.34] \times VCC$$



CPU FAN Connector

PWM FOR EC



PWM FAN

LINEAR FAN

PIN1 PWM
PIN2 GND
PIN3 FG
PIN4 VCC

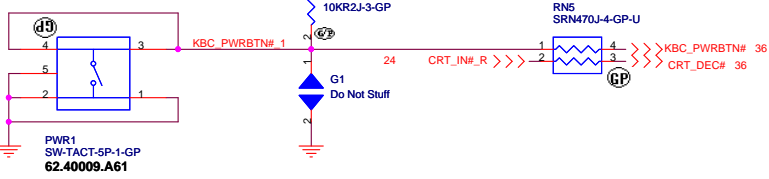
PIN1 NC
PIN2 GND
PIN3 FG
PIN4 VCC

JV10 CS

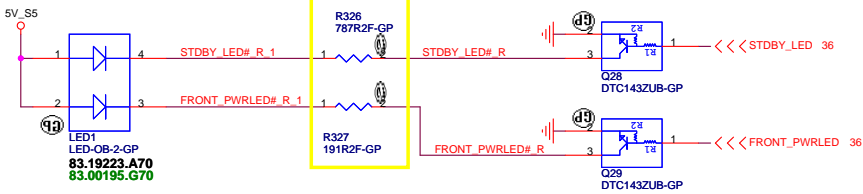
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| Title | | |
|--------------------------------|-----------------|-------|
| Thermal/Fan Conn | | |
| Size A3 | Document Number | Rev |
| | JV10-CS | -1 |
| Date: Friday, January 22, 2010 | Sheet 26 | of 50 |

Power Button



Power Button LED (BLUE/ORANGE)



To USBCN1 Connector

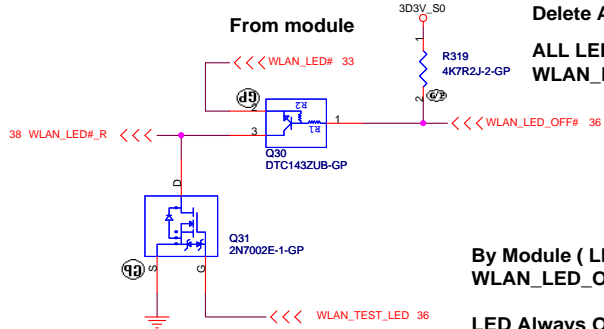
38 STDBY_LED#_R
38 FRONT_PWRLED#_R

From KBC

Delete ALL LED OFF

ALL LED OFF GPIO14 change WLAN_LED
WLAN_LED GPIO81 change WLAN_TEST_LED

From module

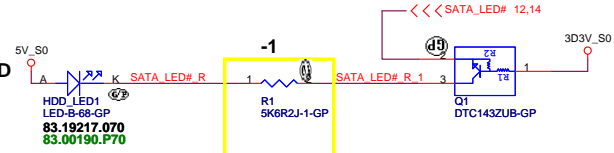


By Module (LED Flash)
WLAN_LED_OFF# High

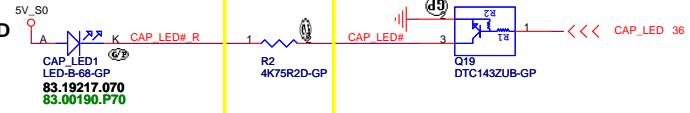
LED Always On
WLAN_LED_OFF# Low
WLAN_TEST_LED High

Factory test use
WLAN_TEST_LED High

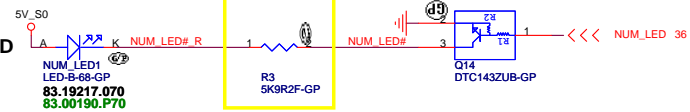
HDD LED (BLUE)



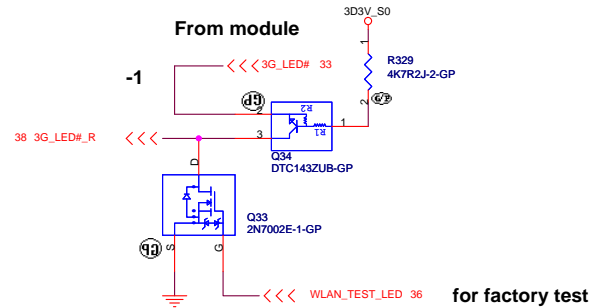
CAP LED (BLUE)



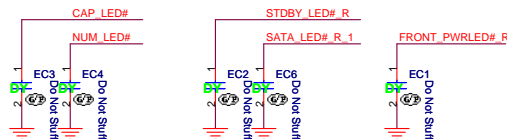
NUM LED (BLUE)



From module



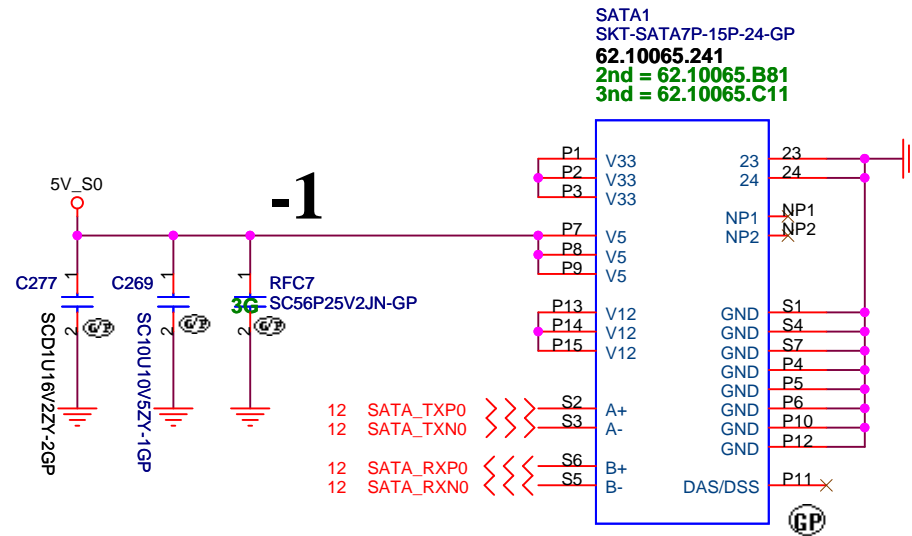
for factory test



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| | |
|--|--------------------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| LED | |
| Size | Document Number |
| Custom | JV10-CS |
| Date: | Friday, January 22, 2010 |
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| Rev | -1 |

SATA Connector



JV10 CS

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Title

HDD

Size
A4

Document Number

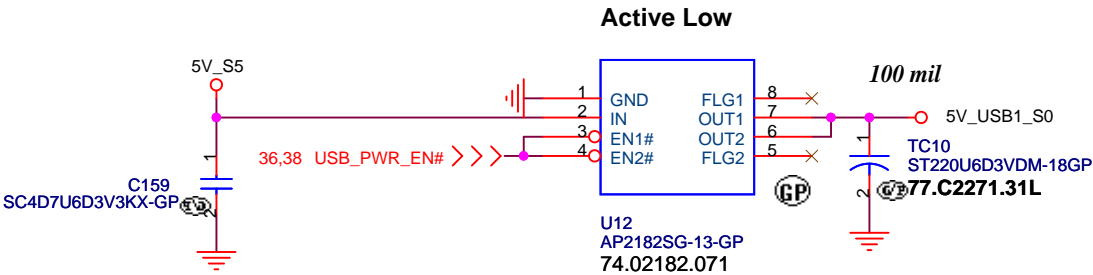
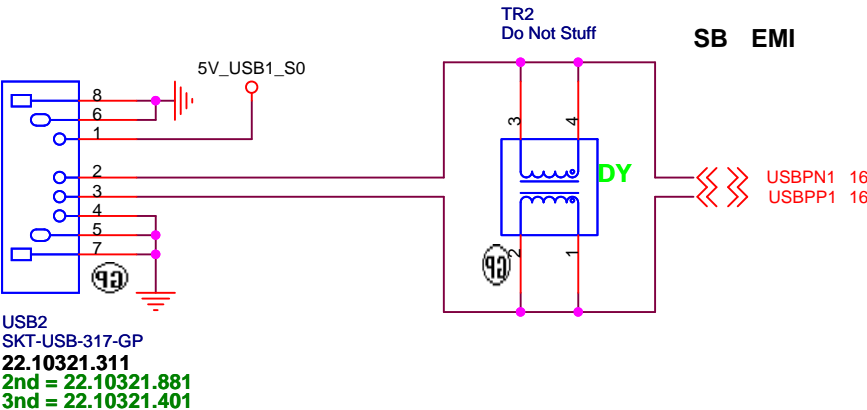
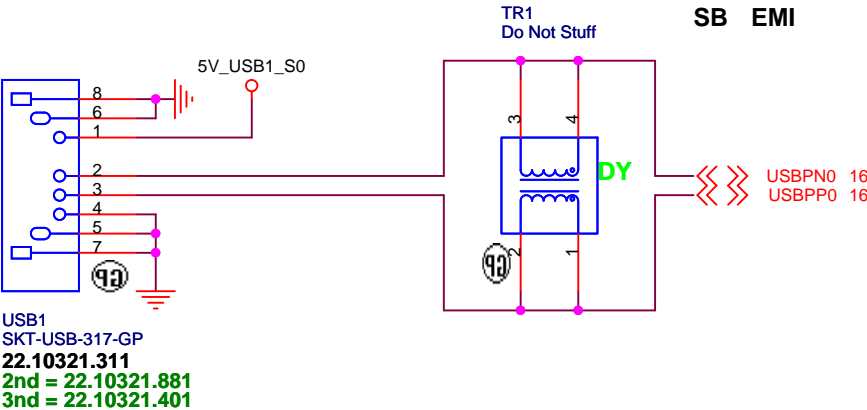
JV10-CS

Rev
-1

Date: Friday, January 22, 2010

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USB MODULE



JV10 CS

| | | | |
|-----------------|-----------------------------------|---|------------------|
| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| USB Port | | | |
| Size A4 | Document Number JV10-CS | | Rev -1 |
| Date: | Friday, January 22, 2010 | Sheet 29 of | 50 |

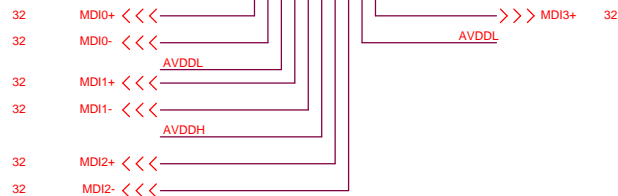
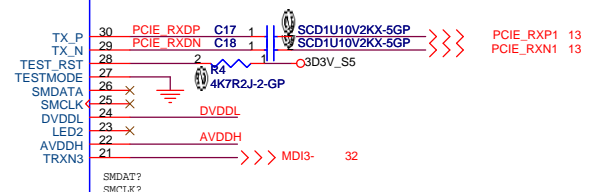
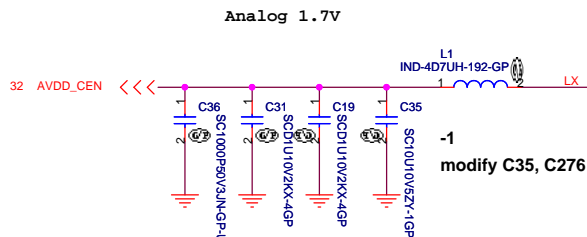
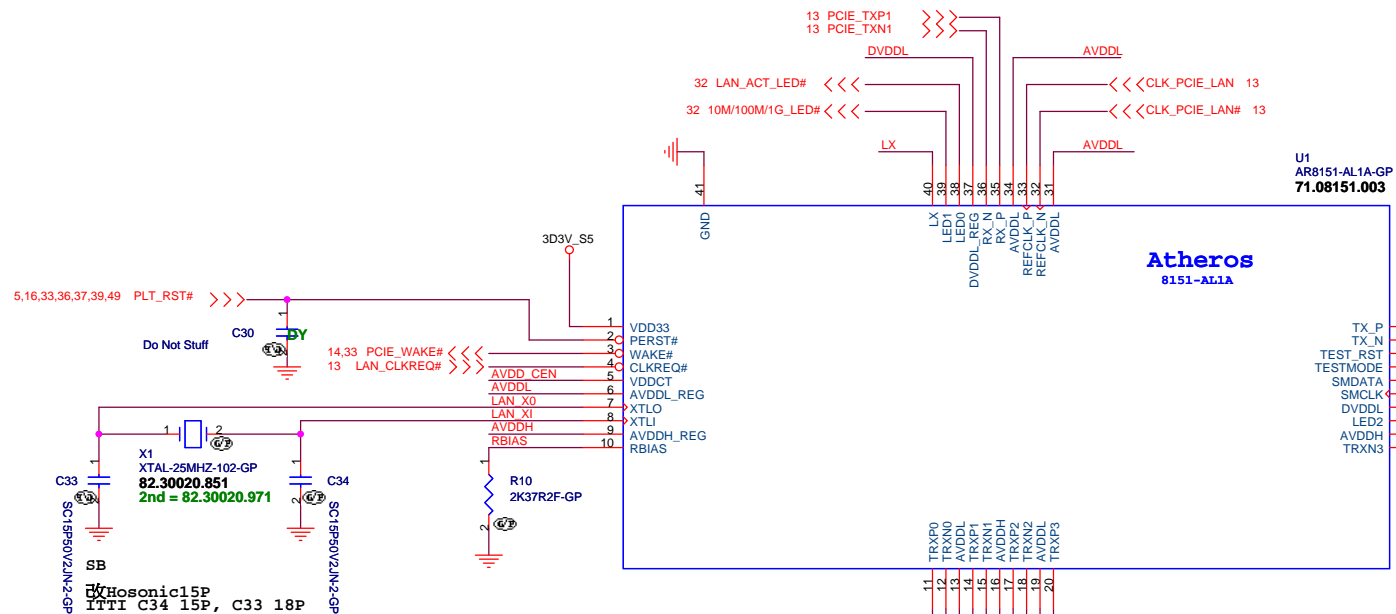
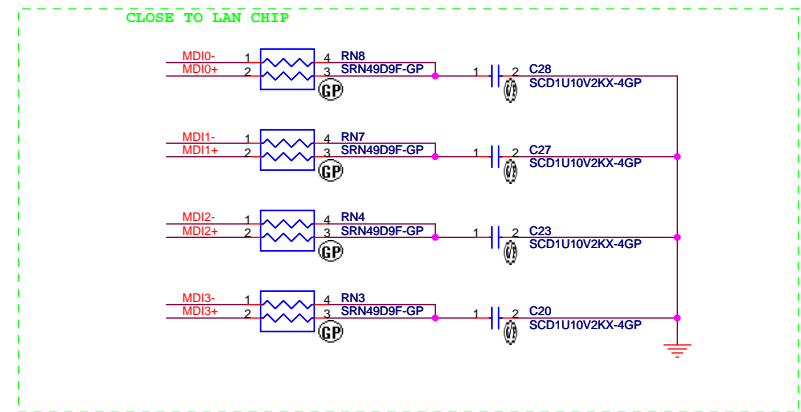
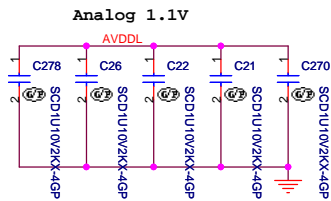
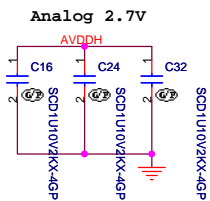
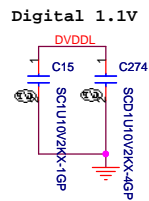
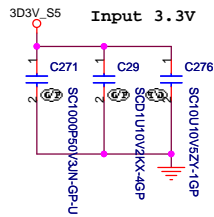
SB 與 ALPS Co-Layout



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|------------|----------------------------|-----------|
| Size A4 | Document Number JV10-CS | Rev -1 |
|------------|----------------------------|-----------|

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|--------------------------------|----------------|
| Date: Friday, January 22, 2010 | Sheet 30 of 50 |
|--------------------------------|----------------|



JV10 CS

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Title AR8151 chip

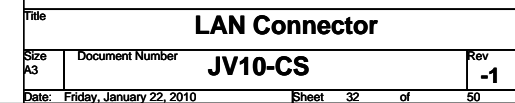
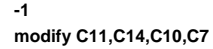
Size A3 Document Number JV10-CS Rev -1

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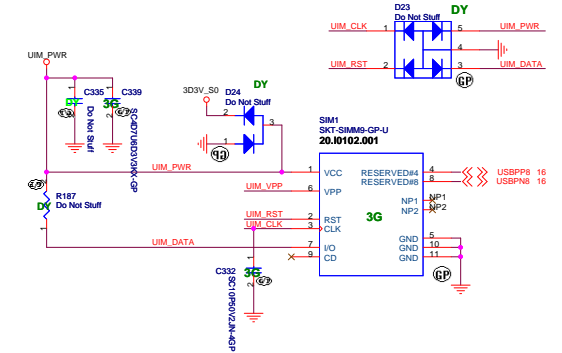
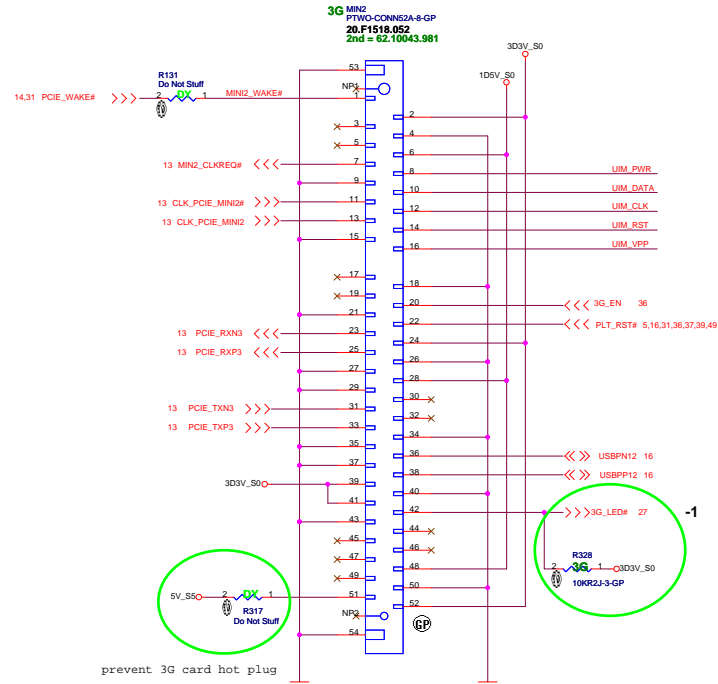
- A

1

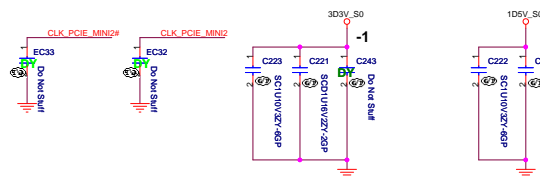
WWW.AliSaler.Com



Mini Card Connector(3G)

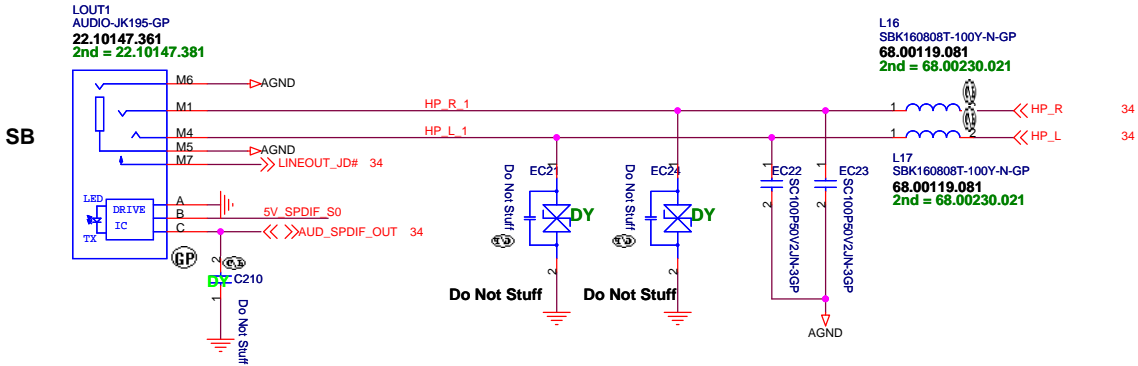


Place near MINIC2

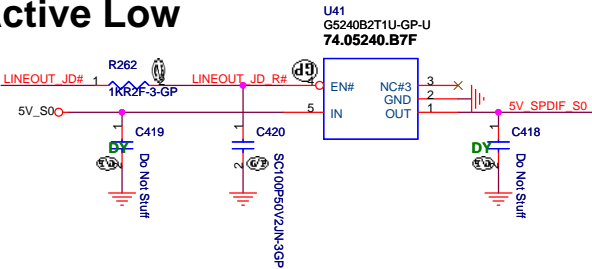


| | | | |
|--------------------------------|-----------------|--|----|
| JV10 CS | | 緯創資通 Wistron Corporation 21F, 86, Sec. 1, Hsin Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C. | |
| File | | MINI Conn | |
| Size Custom | Document Number | JV10-CS Rev -1 | |
| Date: Friday, January 22, 2010 | Sheet 33 | of | 50 |

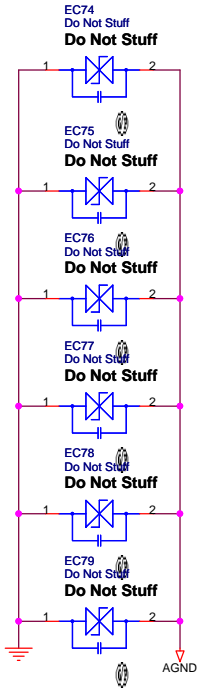
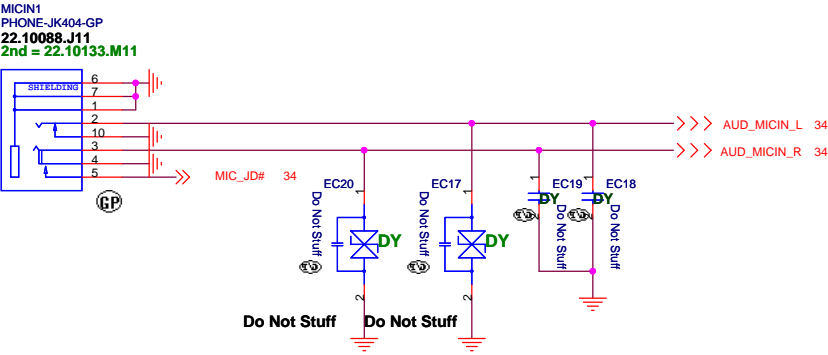
LINE OUT



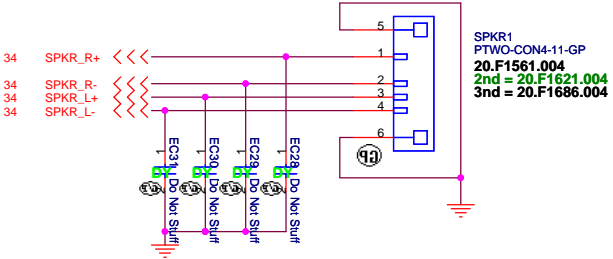
Active Low

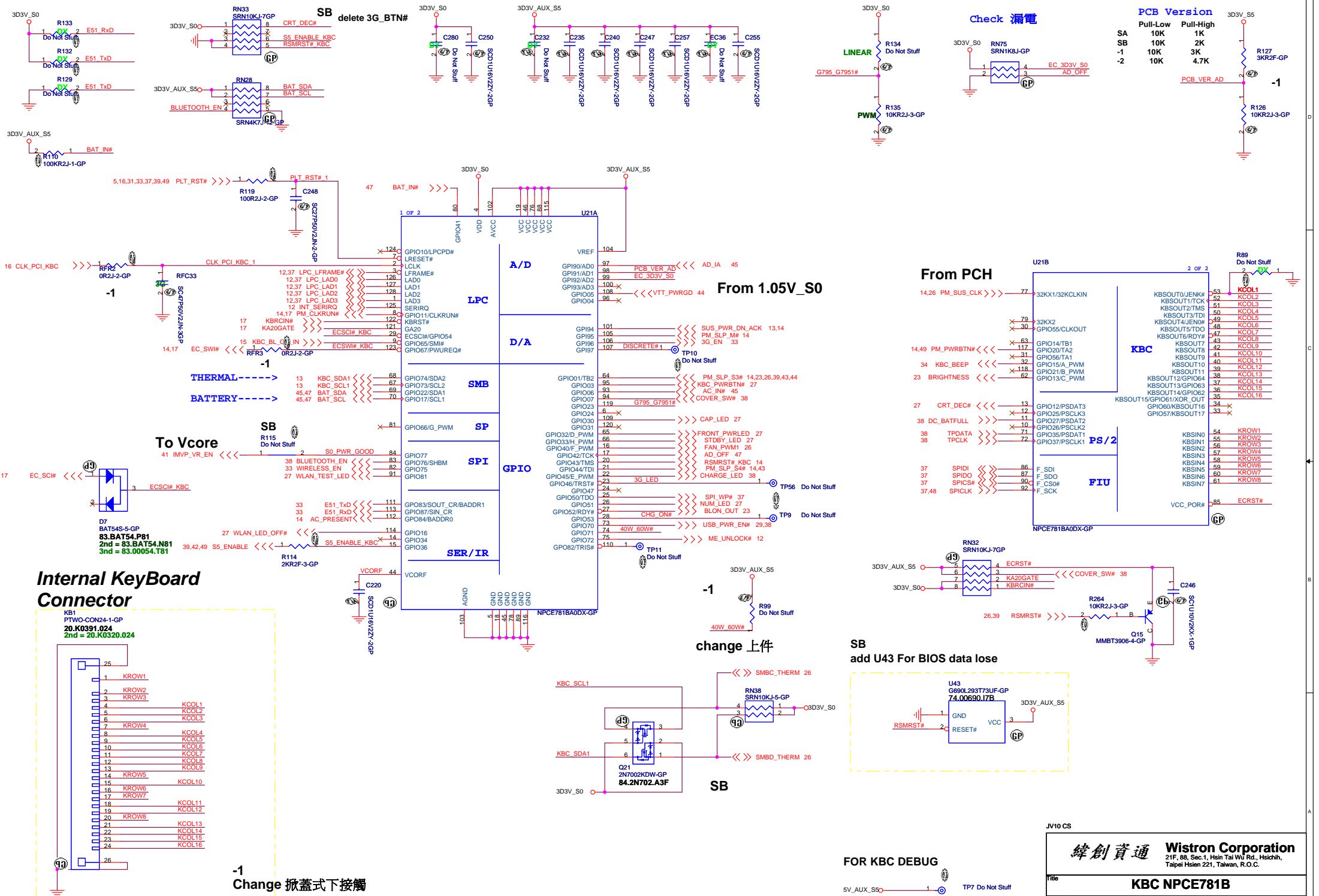


MIC IN

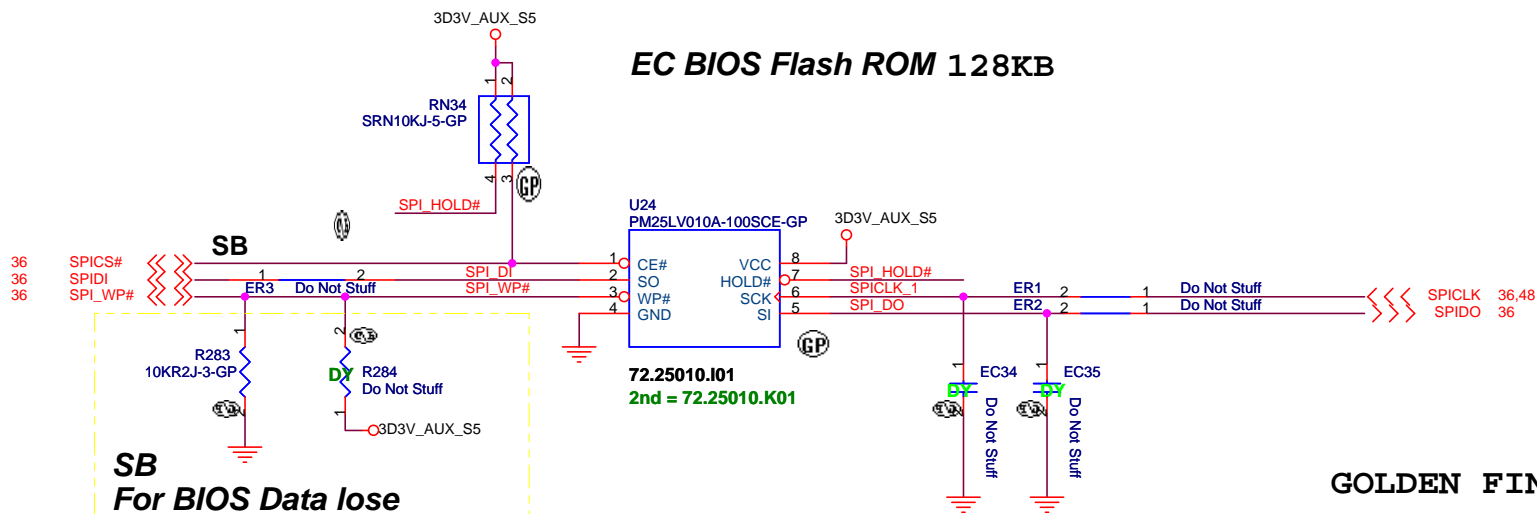


Internal Speaker

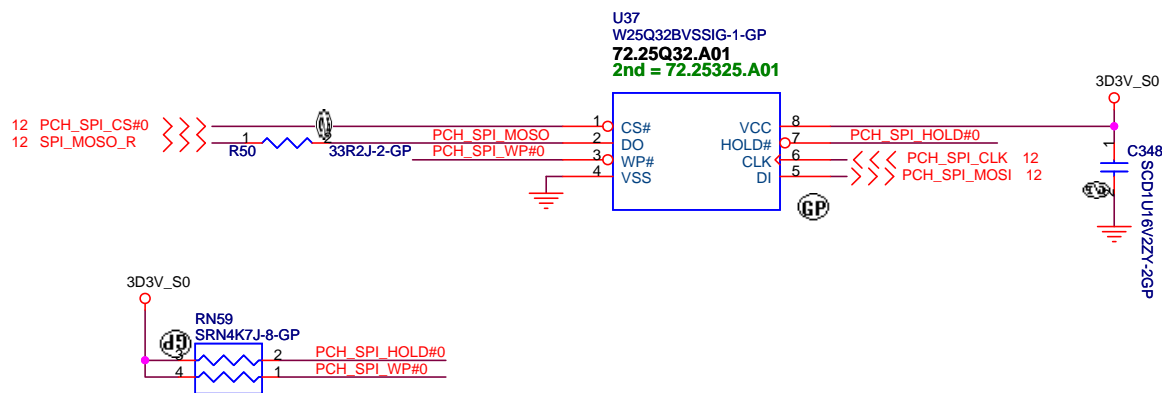




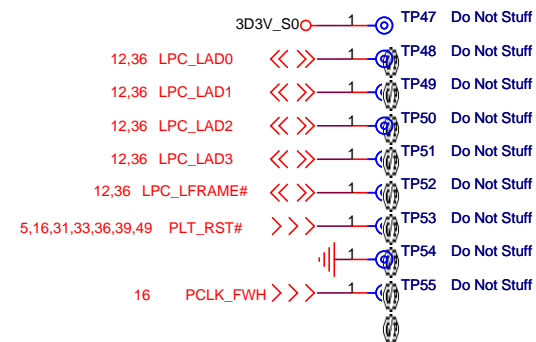
EC BIOS Flash ROM 128KB



System BIOS Flash ROM 4MB



GOLDEN FINGER FOR DEBUG BOARD



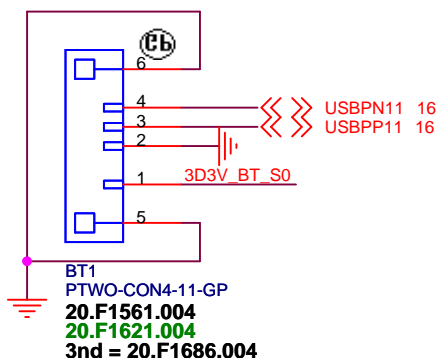
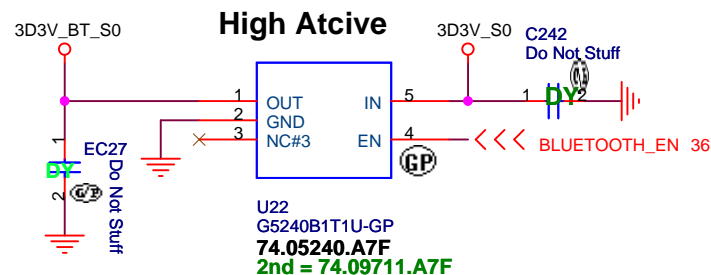
JV10 CS

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|--------|--------------------------|------------------|----------|
| Title | | BIOS | |
| Size | Document Number | JV10-CS | |
| Custom | | Rev -1 | |
| Date: | Friday, January 22, 2010 | Sheet | 37 of 50 |

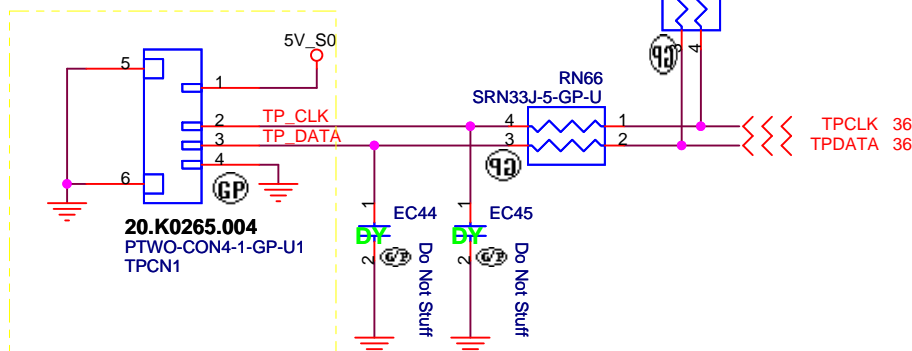
BLUETOOTH Connector



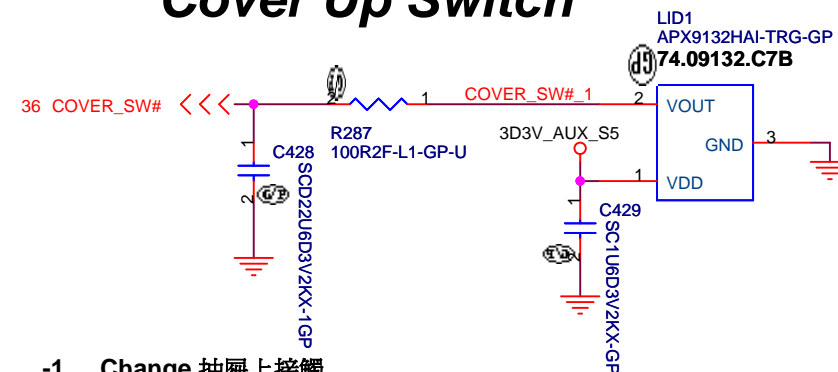
TOUCH PAD Connector

-1 Pin SWAP

Change 抽屜上接觸 異面

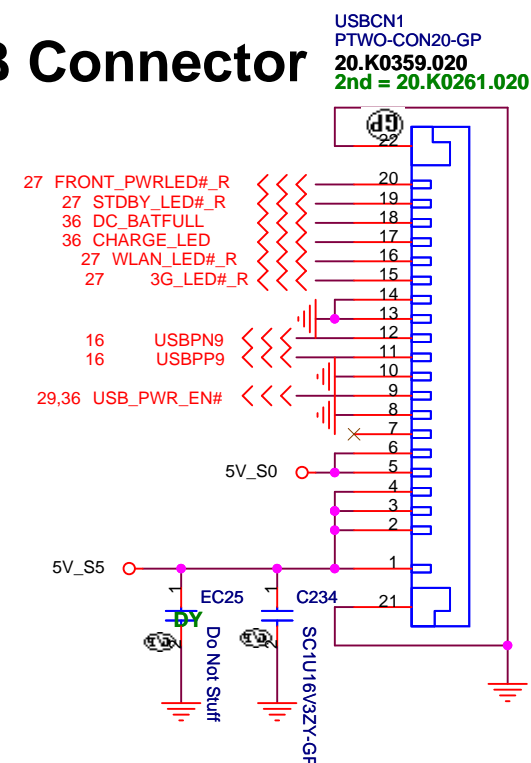


Cover Up Switch



-1 Change 抽屜上接觸

USB Connector



JV10 CS

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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CONNECTOR

Size

Document Number

JV10-CS

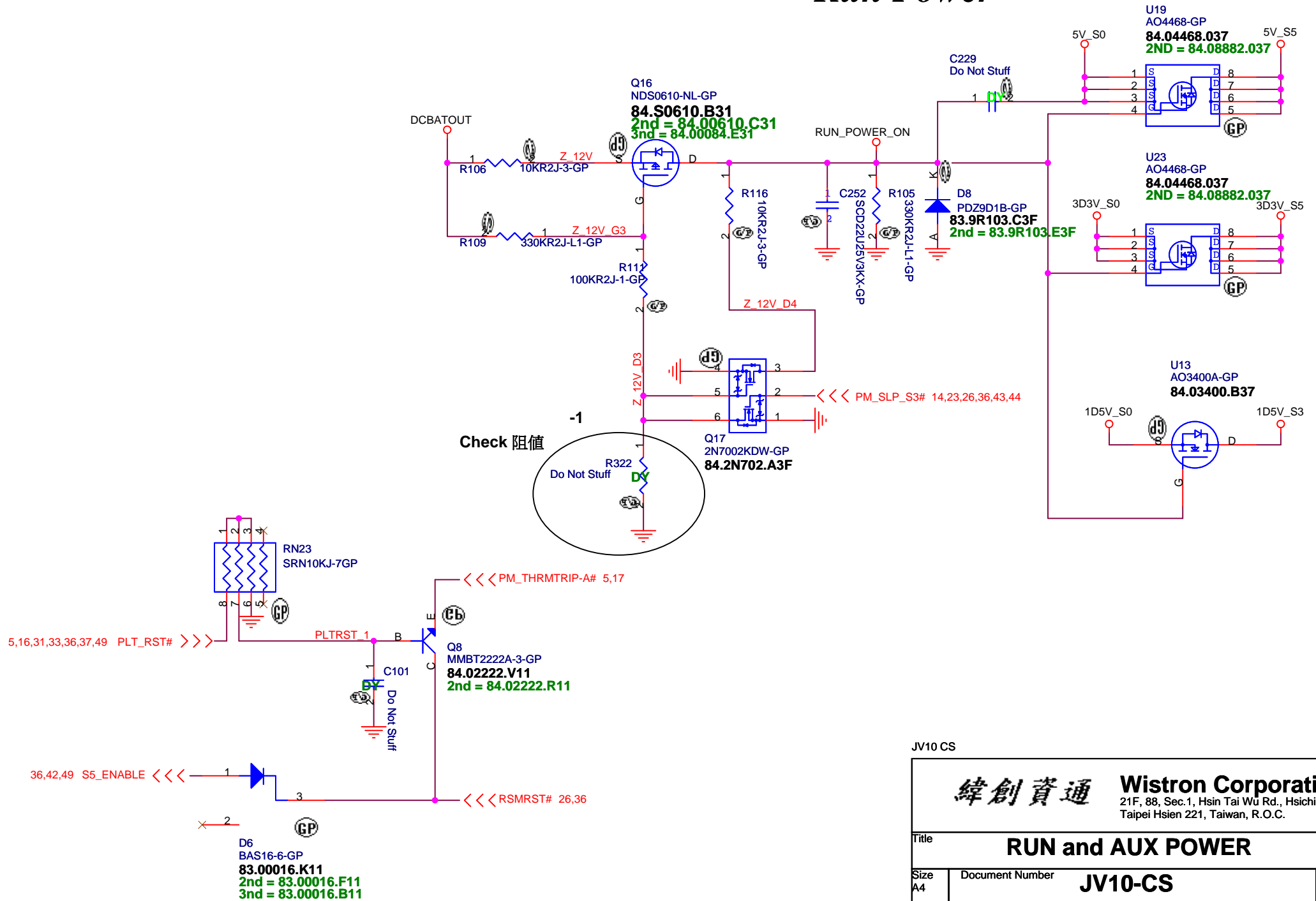
Rev

-1

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Run Power



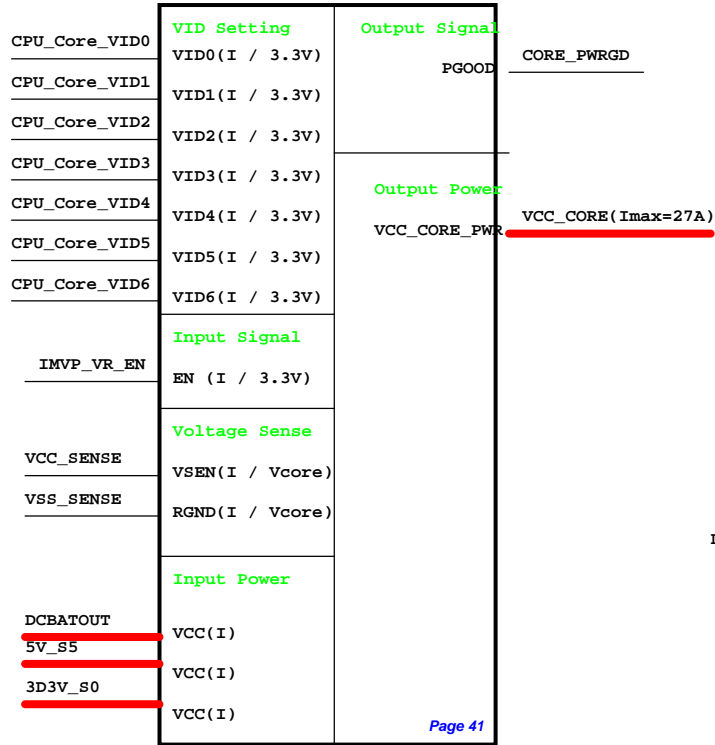
JV10 CS

緯創資通

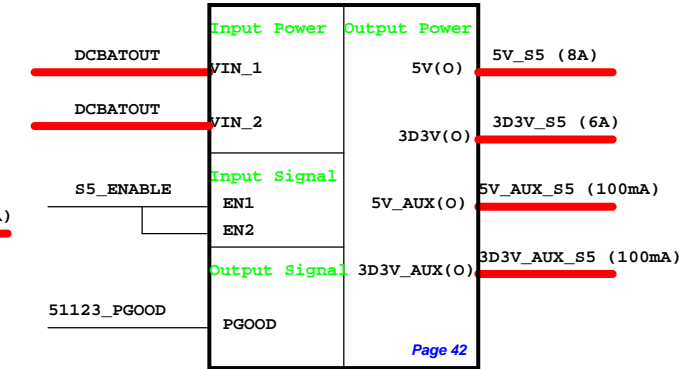
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| Title | | |
|--------------------------------|-----------------|----------------|
| RUN and AUX POWER | | |
| Size | Document Number | Rev |
| A4 | JV10-CS | -1 |
| Date: Friday, January 22, 2010 | | Sheet 39 of 50 |

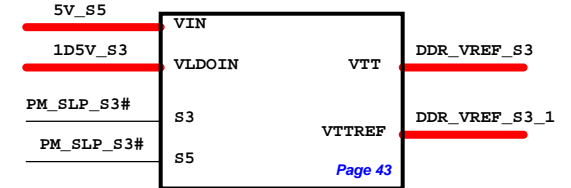
TPS51611 VCC_CORE



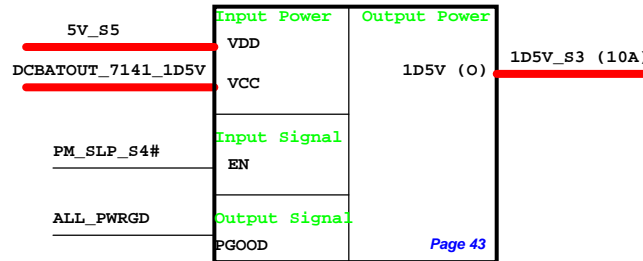
RT8223 5V/3D3V_S5



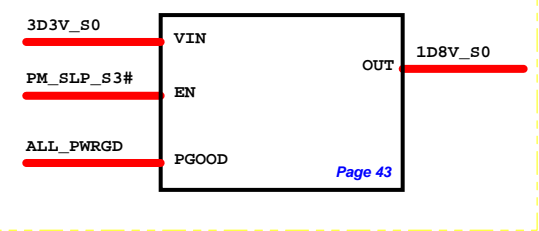
RT9026 DDR_VREF_S3



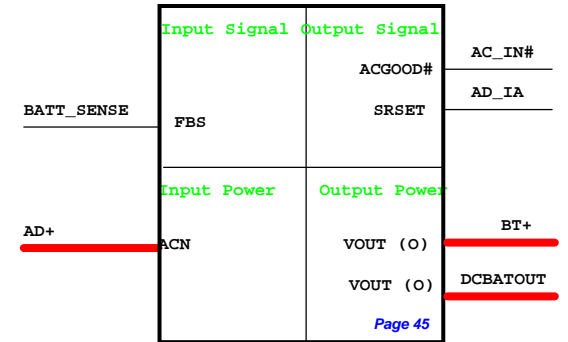
RT8209E 1D5V_S3



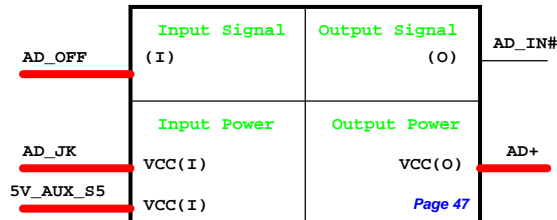
RT9025 1D8V_S0



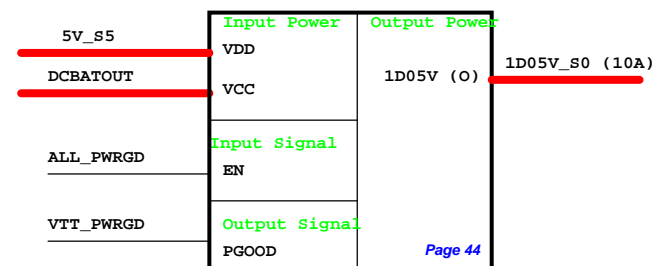
Charger ISL88731A



Adapter



RT8209B 1D05V

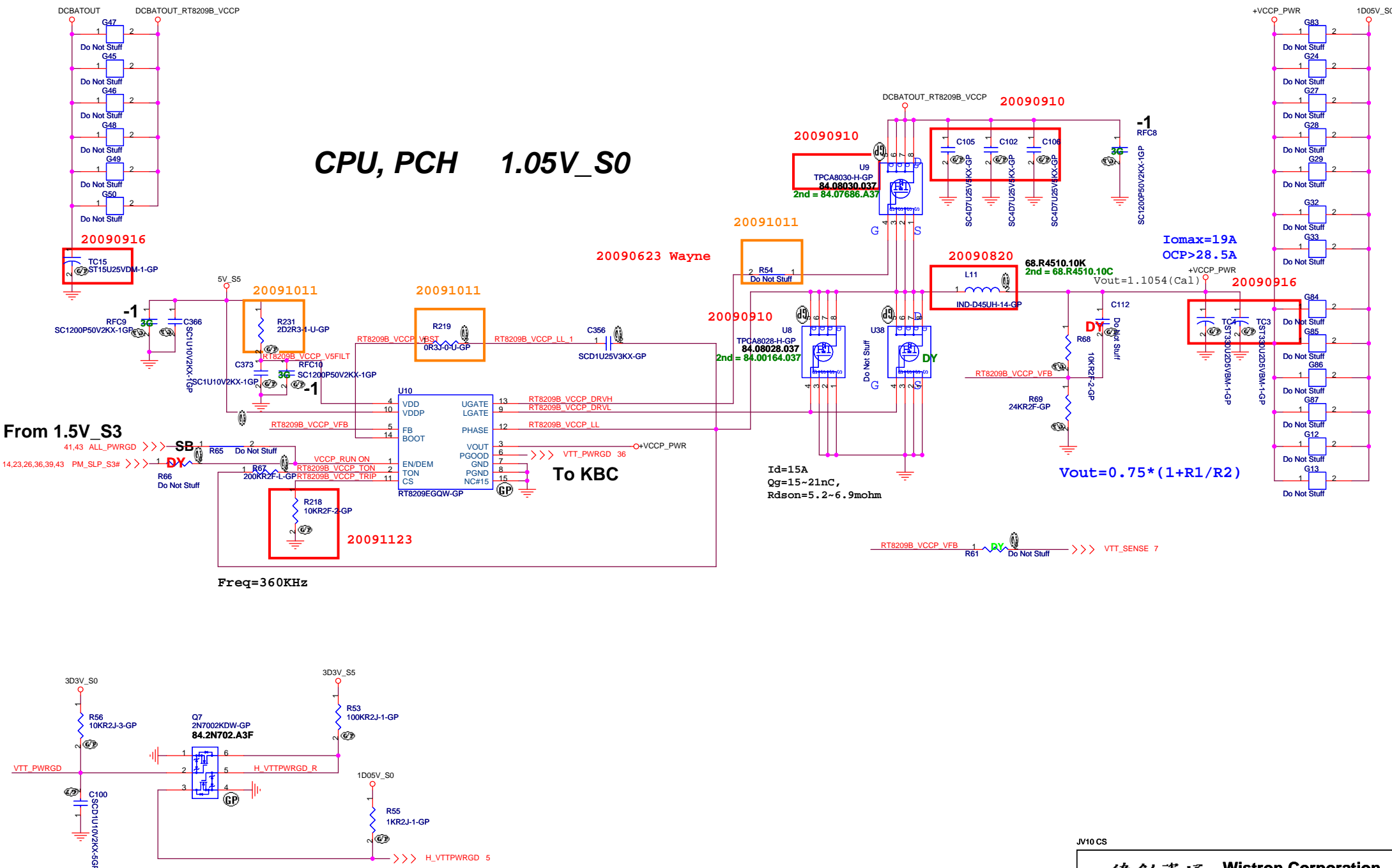


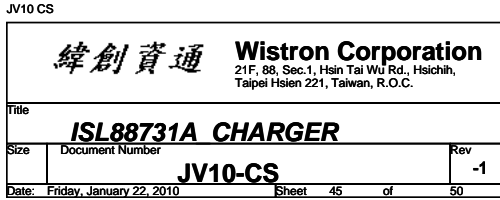
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Taipei Hsien 221, Taiwan, R.O.C.

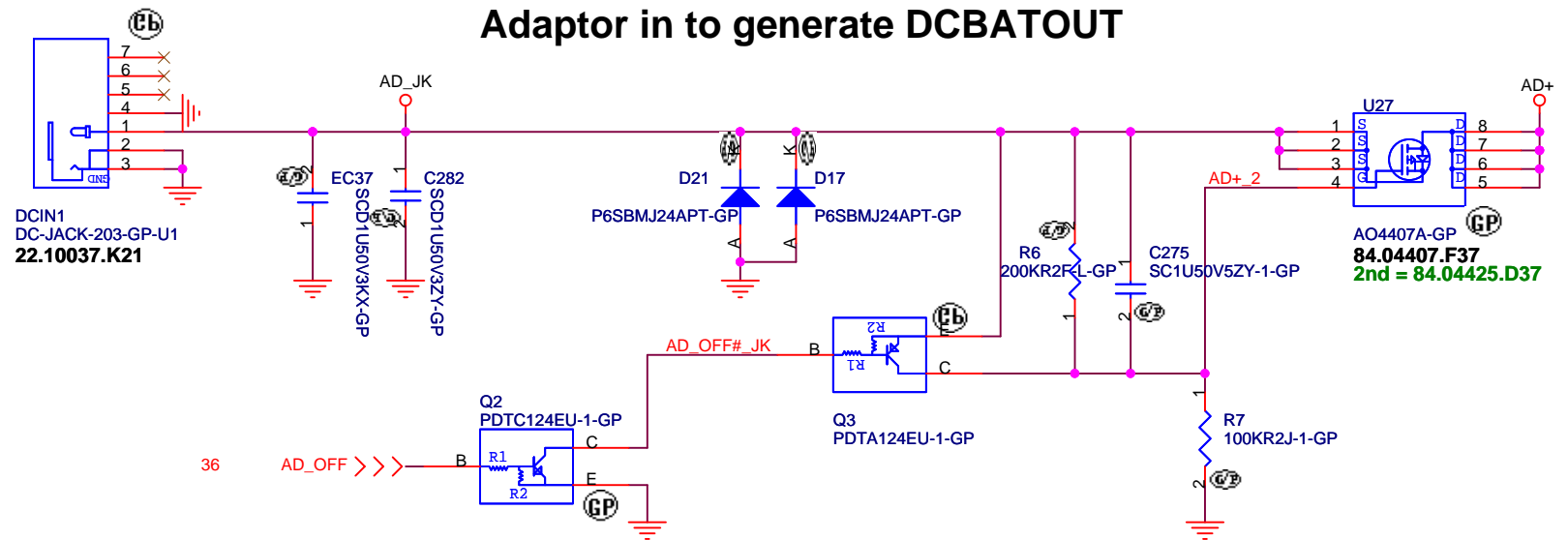
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| Title Power Block Diagram | | | |
| Size | Document Number | JV10-CS | Rev -1 |
| Date: Friday, January 22, 2010 | Sheet 40 | of 50 | |

CPU, PCH 1.05V_S0

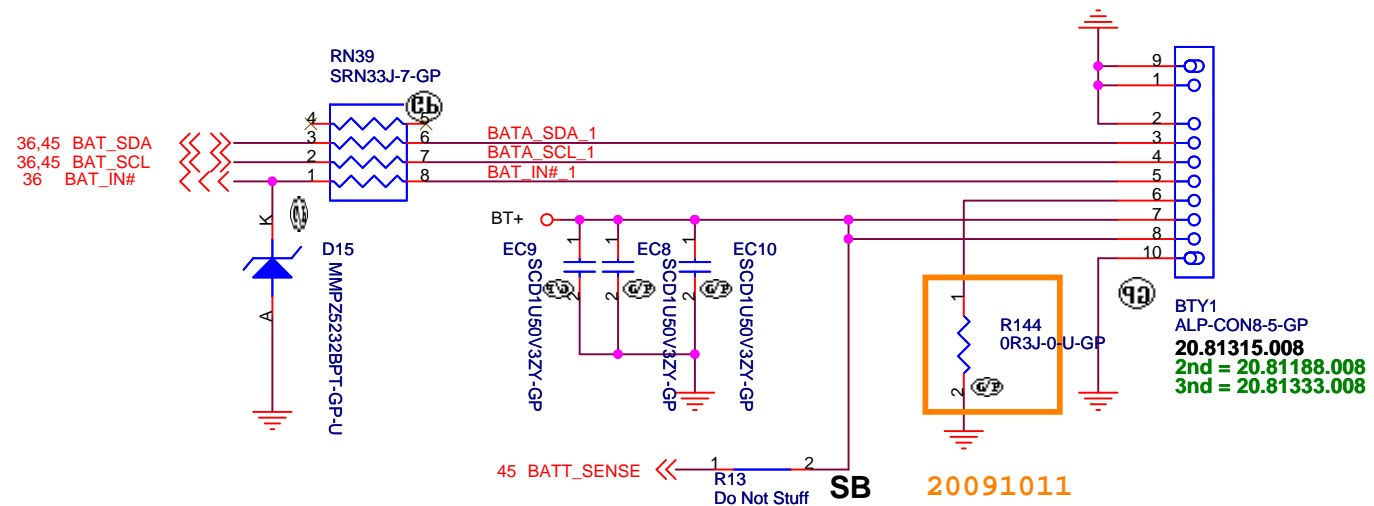




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title

AD/BATT CONN

Size

Document Number

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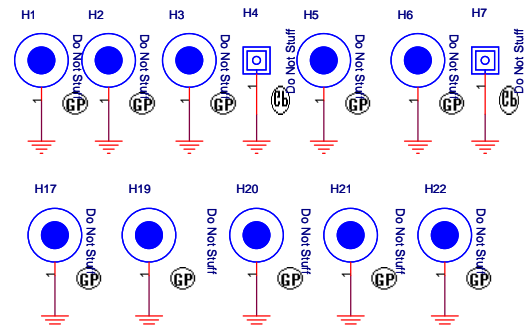
Rev

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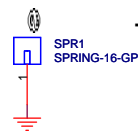
Date: Friday, January 22, 2010

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MB HOLE



SPRING



MINI CARD BOSS

(BTN Side)

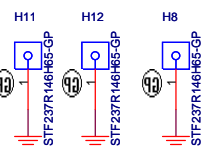
HALF MINI CARD

FULL MINI CARD

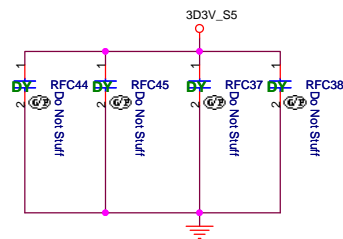


CPU PCH BOSS

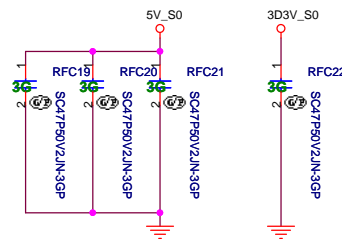
(BTN Side)



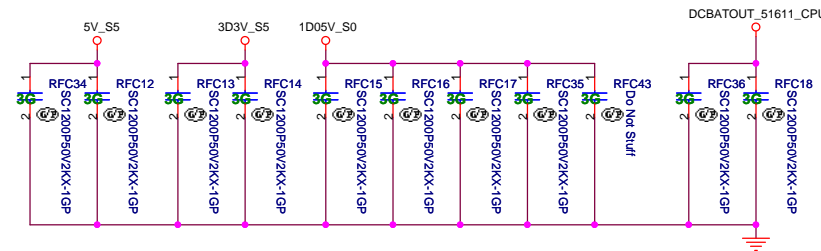
For RF power point Page 26



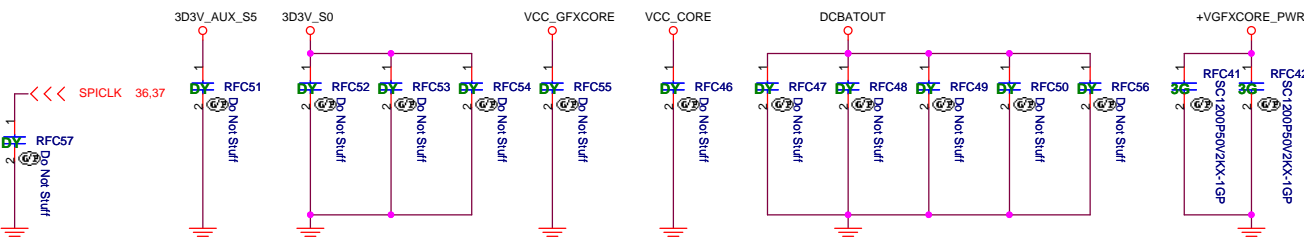
For RF power point Page 12



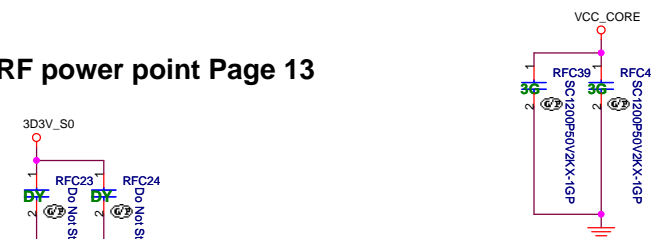
For RF power point Page 4



For RF power point Page 17

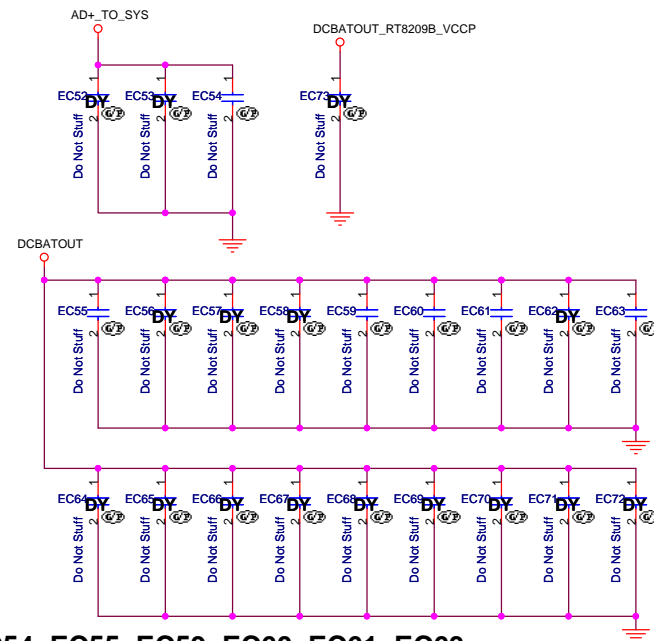


For RF power point Page 13



SB

EMI



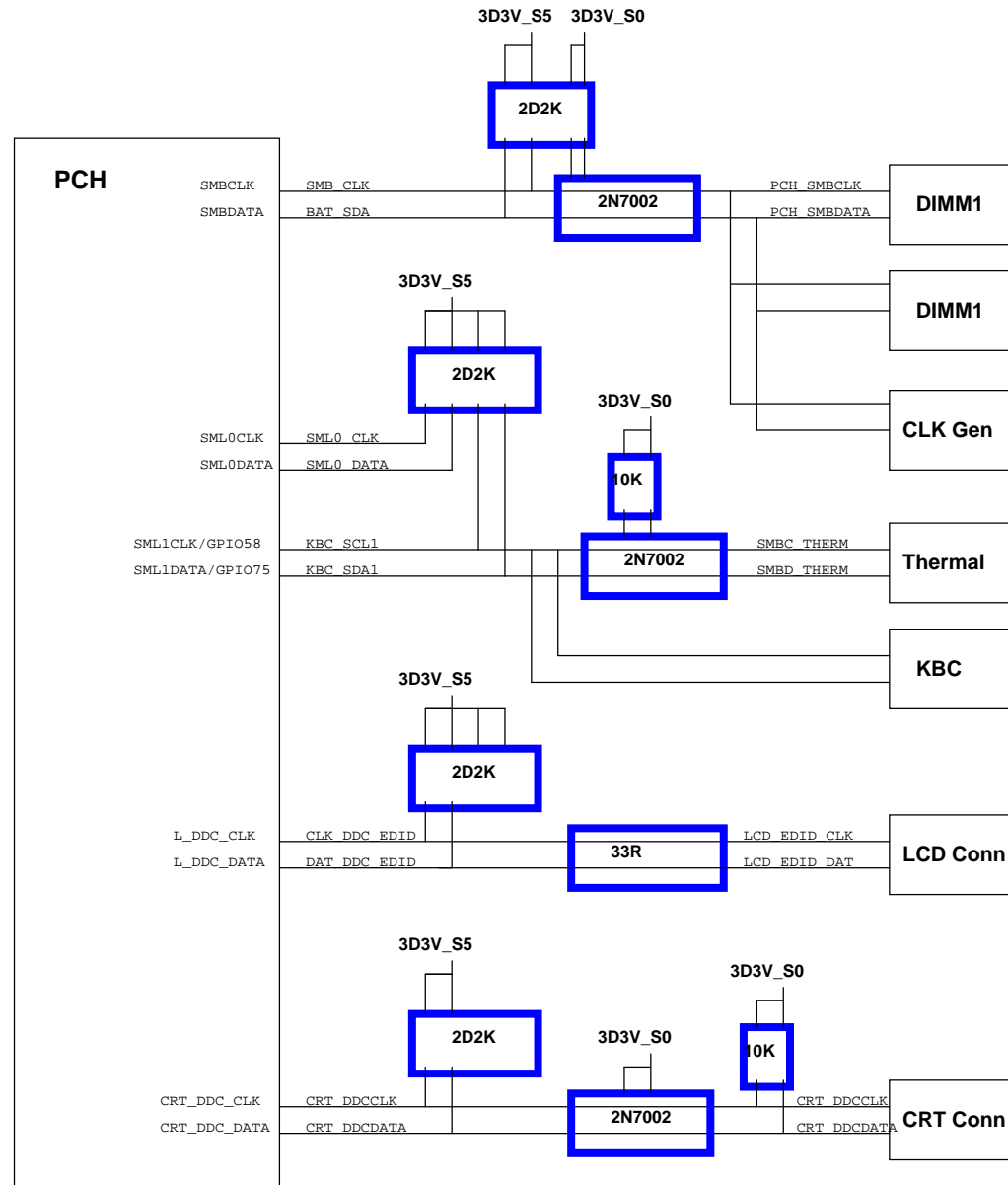
EC54, EC55, EC59, EC60, EC61, EC63

JV10 CS

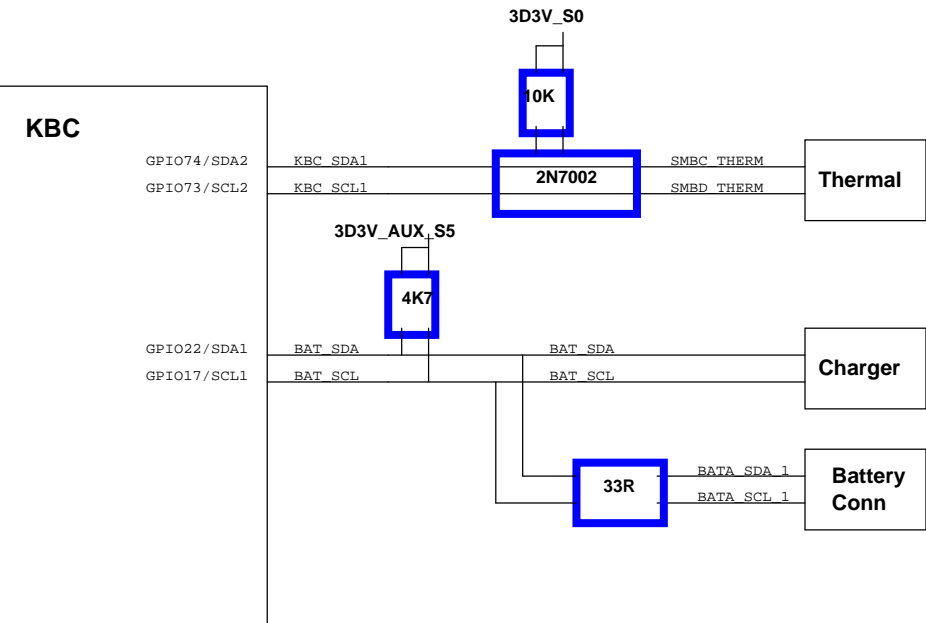
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|-------|--------------------------|-----------------|----------|
| Title | | EMI/Spring/Boss | |
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| Date: | Friday, January 22, 2010 | Sheet | 48 of 50 |

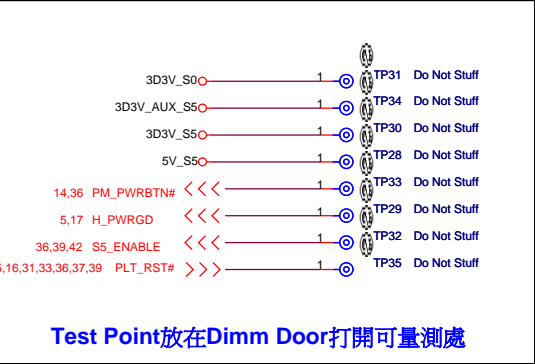
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Check test point



Test Point 放在Dimm Door打開可量測處

SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

- EC SB11/04 add Intel support POC Function(power on current).
- EC SB11/04 SWAP Touch Pad Pin define
- EC SB11/04 R230 add 1K
- EC SB11/04 change LOUT1 part number
- EC SB11/11 SWAP Digital Mic DATA/CLK Pin define
- EC SB11/11 Delete 3G_BTN#,Wireless_BTN#, function
- EC SB11/11 add Cover switch to MB
- EC SB11/11 add RN72 22ohm for Mic in
- EC SB11/16 change U40 1D8V_S0 power solution
- EC SB11/19 modify all LED off Function
- EC SB11/19 change HDD Connector Type
- EC SB11/19 Close Powert team Gap
- EC PD 01/11 modify keyborad connector KB1
- EC PD 01/11 modify USB Touch pad connector TPCN1 USBCN1
- EC PD 01/11 add 3G module LED Function
- EC PD 01/11 EMI add EC54, EC55, EC59, EC60, EC61, EC63, C37
- EC PD 01/11 TPCN1 SWAP Pin define

| | | |
|---|-------------------------|--------|
| JV10 CS | | |
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| Title Modify History | | |
| Size A3 | Document Number JV10-CS | Rev -1 |
| Date: Friday, January 22, 2010 | Sheet 50 of | 50 |